# Si5315

**PRELIMINARY DATA SHEET**

# SYNCHRONOUS ETHERNET/TELECOM JITTER ATTENUATING CLOCK MULTIPLIER

## Features

- Provides jitter attenuation and frequency translation between SONET/PDH and Ethernet
- Supports ITU-T G.8262 Synchronous Ethernet equipment slave clocks (EEC option 1 and 2) requirements
- Two clock inputs/two clock outputs
- Input frequency range: 8 kHz–644 MHz
- Output frequency range: 8 kHz–644 MHz
- Very low jitter: 0.6 ps (12 kHz–20 MHz)
- Simple pin control interface
- Selectable loop bandwidth for jitter attenuation: 60 to 8.4 kHz
- Automatic/Manual hitless reference switching and holdover during loss of reference inputs clock
- Programmable output clock signal format: LVPECL, LVDS, CML or CMOS
- 40 MHz crystal or XO reference
- Single supply: 1.8, 2.5, or 3.3 V
- Loss of lock and loss of signal alarms
- Small size: 6 x 6 mm, 36-QFN
- Wide temperature range: –40 to +85 ºC

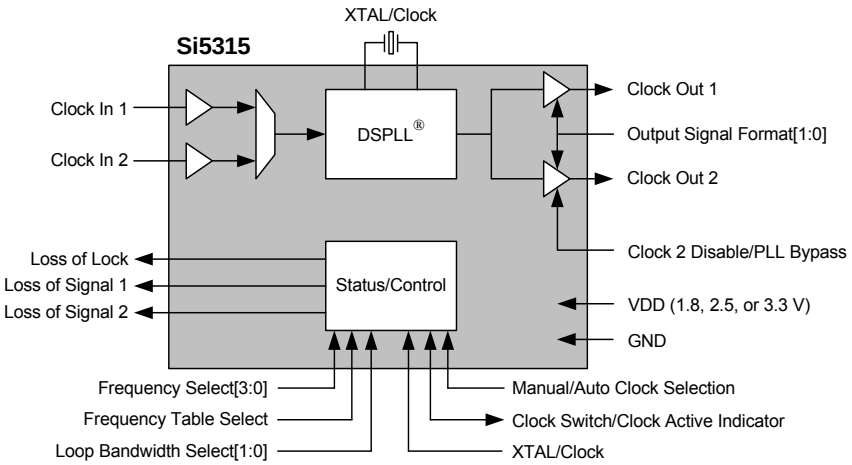
## Applications

- Synchronous Ethernet Line Cards
- SONET OC-3/12/48 Line Cards
- GPON OLT/ONU
- Carrier Ethernet Switches Routers
- DSLAM
- T1/E1/DS3/E3 Line Cards

## Description

The Si5315 is a jitter-attenuating clock multiplier for Gb and 10G Synchronous Ethernet, SONET/SDH, and PDH (T1/E1) applications. The Si5315 accepts dual clock inputs ranging from 8 kHz to 644.53 MHz and generates two equal frequency-multiplied clock outputs ranging from 8 kHz to 644.53 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SyncE and T1/E1 rates. The Si5315 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is user programmable, providing jitter performance optimization at the application level.

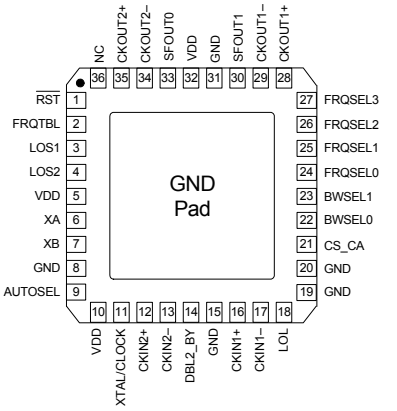
## Functional Block Diagram



**Ordering Information:**

See page 51.

**Pin Assignments**





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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

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# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature Range | $T_A$ | | –40 | 25 | 85 | ºC |
| Supply Voltage | $V_{DD}$ | 3.3 V nominal | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V nominal | 2.25 | 2.5 | 2.75 | V |
| | | 1.8 V nominal | 1.71 | 1.8 | 1.89 | V |

**Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

### Table 2. DC Characteristics

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Current (Supply current is independent of $V_{DD}$) | $I_{DD}$ | LVPECL Format 644.53125 MHz Out All CKOUTs Enabled[1] | — | 251 | 279 | mA |
| | | LVPECL Format 644.53125 MHz Out Only 1 CKOUT Enabled[1] | — | 253 | 284 | mA |
| | | CMOS Format 125.00 MHz Out All CKOUTs Enabled[2] | — | 204 | 234 | mA |
| | | CMOS Format 125.00 MHz Out Only CKOUT1 Enabled[2] | — | 194 | 220 | mA |
| **CKINn Input Pins** | | | | | | |
| Input Common Mode Voltage (Input Threshold Voltage) | $V_{ICM}$ | 1.8 V ± 10% | 0.9 | — | 1.4 | V |
| | | 2.5 V ± 10% | 1.0 | — | 1.7 | V |
| | | 3.3 V ± 10% | 1.1 | — | 1.95 | V |
| Input Resistance | $CKN_{RIN}$ | Single-ended | 20 | 40 | 60 | kΩ |
| Input Voltage Level Limits | $CKN_{VIN}$ | | 0 | — | $V_{DD}$ | V |
| Single-Ended Input Voltage Swing | $V_{ISE}$ | $f_{CKIN} \le$ 212.5 MHz See Figure 2. | 0.2 | — | — | $V_{PP}$ |
| | | $f_{CKIN}$ > 212.5 MHz See Figure 2. | 0.25 | — | — | $V_{PP}$ |

**Notes:**
1. Refers to Si5315A speed grade.
2. Refers to Si5315B speed grade.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Differential Input Voltage Swing | $V_{ID}$ | $f_{CKIN} \leq$ 212.5 MHz See Figure 2. | 0.2 | — | 1.9 | $V_{PP}$ |
| | | $f_{CKIN}$ > 212.5 MHz See Figure 2. | 0.25 | — | 1.9 | $V_{PP}$ |
| **CKOUTn Output Clocks** | | | | | | |
| Common Mode | $V_{OCM}$ | LVPECL 100 Ω load line-to-line | $V_{DD}$ – 1.42 | — | $V_{DD}$ – 1.25 | V |
| Differential Output Swing | $V_{OD}$ | LVPECL 100 Ω load line-to-line | 1.1 | — | 1.9 | $V_{PP}$ |
| Single Ended Output Swing | $V_{SE}$ | LVPECL 100 Ω load line-to-line | 0.5 | — | 0.93 | $V_{PP}$ |
| Differential Output Voltage | $CKO_{VD}$ | CML 100 Ω load line-to-line | 350 | 425 | 500 | $mV_{PP}$ |
| Common Mode Output Voltage | $CKO_{VCM}$ | CML 100 Ω load line-to-line | — | $V_{DD}$ – 0.36 | — | V |
| Differential Output Voltage | $CKO_{VD}$ | LVDS 100 Ω load line-to-line | 500 | 700 | 900 | $mV_{PP}$ |
| | | Low swing LVDS 100 Ω load line-to-line | 350 | 425 | 500 | $mV_{PP}$ |
| Common Mode Output Voltage | $CKO_{VCM}$ | LVDS 100 Ω load line-to-line | 1.125 | 1.2 | 1.275 | V |
| Output Short to GND | $CKO_{ISC}$ | $V_{DD}$ = 3.63 V CML, LVDS, LVPECL | — | 80 | 90 | mA |
| | | $V_{DD}$ = 1.89 V CML, LVDS | — | 45 | 50 | mA |
| | | $V_{DD}$ = 3.63 V CMOS | — | 165 | 175 | mA |
| | | $V_{DD}$ = 1.89 V CMOS | — | 65 | 70 | mA |
| | | Disable | — | 0.1 | 0.2 | µA |

**Notes:**
1. Refers to Si5315A speed grade.
2. Refers to Si5315B speed grade.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9.

**Table 2. DC Characteristics (Continued)**

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output Short to $V_{DD}$ | $CKO_{ISC+}$ | $V_{DD}$ = 3.63 V CML, LVDS, LVPECL | — | 25 | 30 | mA |
| | | $V_{DD}$ = 1.89 V CML, LVDS | — | 25 | 30 | mA |
| | | $V_{DD}$ = 3.63 V CMOS | — | 190 | 200 | mA |
| | | $V_{DD}$ = 1.89 V CMOS | — | 70 | 80 | mA |
| | | Disable | — | 1.5 | 2 | µA |
| Differential Output Resistance | $CKO_{RD}$ | CML, LVPECL, LVDS, Disable | 170 | 200 | 230 | Ω |
| Common Mode Output Resistance (to $V_{DD}$) | $CKO_{RCM}$ | CML, LVPECL, LVDS | 85 | 100 | 115 | Ω |
| | | Disable | 1 | — | — | MΩ |
| Output Voltage Low | $CKO_{VOLLH}$ | CMOS | — | — | 0.4 | V |
| Output Voltage High | $CKO_{VOHLH}$ | $V_{DD}$ = 1.71 V CMOS | 0.8 x $V_{DD}$ | — | — | V |
| Output Drive Current | $CKO_{IO}$ | CMOS Driving into $CKO_{VOL}$ for output low or $CKO_{VOH}$ for output high. CKOUT+ and CKOUT– shorted externally. | | | | |
| | | $V_{DD}$ = 1.71 V | 7.5 | — | — | mA |
| | | $V_{DD}$ = 2.97 V | 32 | — | — | mA |
| **2-Level LVCMOS Input Pins** | | | | | | |
| Input Voltage Low | $V_{IL}$ | $V_{DD}$ = 1.71 V | — | — | 0.5 | V |
| | | $V_{DD}$ = 2.25 V | — | — | TBD | V |
| | | $V_{DD}$ = 2.97 V | — | — | 0.8 | V |
| Input Voltage High | $V_{IH}$ | $V_{DD}$ = 1.89 V | 1.4 | — | — | V |
| | | $V_{DD}$ = 2.25 V | TBD | — | — | V |
| | | $V_{DD}$ = 3.63 V | 2.5 | — | — | V |
| Input Low Current | $I_{IL}$ | | — | — | 50 | µA |
| Input High Current | $I_{IH}$ | | — | — | 50 | µA |
| Weak Internal Input Pullup Resistor | $R_{PUP}$ | | — | 24.6 | — | kΩ |
| Weak Internal Input Pulldown Resistor | $R_{PDN}$ | | — | 24.6 | — | kΩ |

**Notes:**

1. Refers to Si5315A speed grade.
2. Refers to Si5315B speed grade.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **3-Level Input Pins** | | | | | | |
| Input Voltage Low | $V_{ILL}$ | | — | — | 0.15 x $V_{DD}$ | V |
| Input Voltage Mid | $V_{IMM}$ | | 0.45 x $V_{DD}$ | — | 0.55 x $V_{DD}$ | V |
| Input Voltage High | $V_{IHH}$ | | 0.85 x $V_{DD}$ | — | — | V |
| Input Low Current | $I_{ILL}$ | See note 3. | –20 | — | — | µA |
| Input Mid Current | $I_{IMM}$ | See note 3. | –2 | — | 2 | µA |
| Input High Current | $I_{IHH}$ | See note 3. | — | — | 20 | µA |
| **LVCMOS Output Pins** | | | | | | |
| Output Voltage Low | $V_{OL}$ | $I_O$ = 2 mA<br>$V_{DD}$ = 1.62 V | — | — | 0.4 | V |
| | | $I_O$ = 2 mA<br>$V_{DD}$ = 2.97 V | — | — | 0.4 | V |
| Output Voltage High | $V_{OH}$ | $I_O$ = –2 mA<br>$V_{DD}$ = 1.62 V | $V_{DD}$ – 0.4 | — | — | V |
| | | $I_O$ = –2 mA<br>$V_{DD}$ = 2.97 V | $V_{DD}$ – 0.4 | — | — | V |
| **Single-Ended Reference Clock Input Pin XA (XB with cap to gnd)** | | | | | | |
| Input Resistance | $XA_{RIN}$ | XTAL/CLOCK = M | 8.5 | 10 | 11.5 | kΩ |
| Input Voltage Level Limits | $XA_{VIN}$ | | 0 | — | 1.2 | V |
| Input Voltage Swing | $XA_{VPP}$ | | 0.5 | — | 1.2 | $V_{PP}$ |
| **Differential Reference Clock Input Pins (XA/XB)** | | | | | | |
| Input Resistance | $XA/XB_{RIN}$ | XTAL/CLOCK = M | 8.5 | 10 | 11.5 | kΩ |
| Differential Input Voltage Level Limits | $XA/XB_{VIN}$ | | 0 | — | 1.2 | V |
| Input Voltage Swing | $XA_{VPP}/XB_{VPP}$ | | 0.5 | — | 1.2 | $V_{PP, each}$ |

**Notes:**
1. Refers to Si5315A speed grade.
2. Refers to Si5315B speed grade.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9.

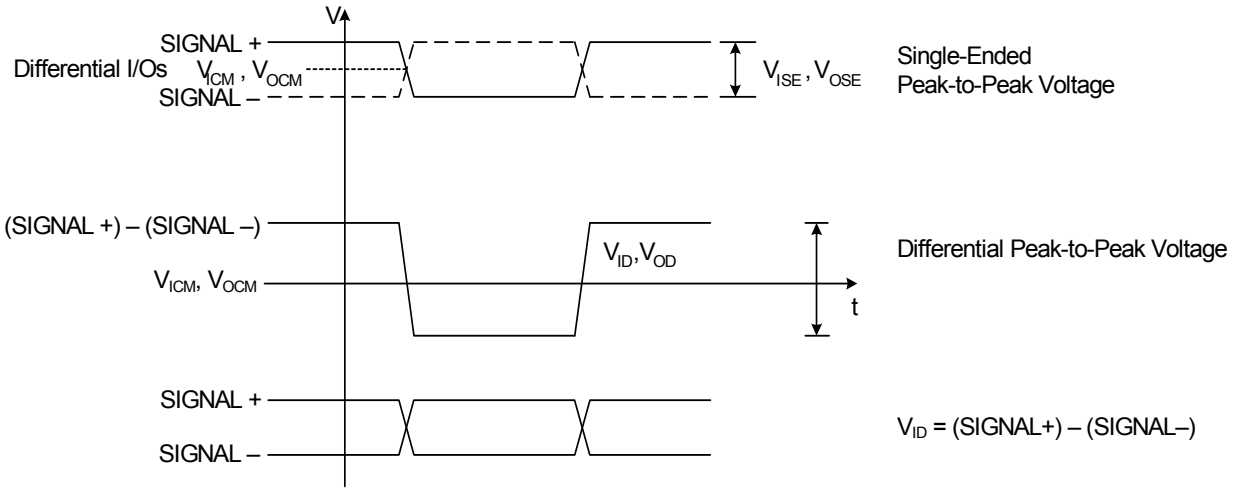



**Figure 1. Differential Voltage Characteristics**

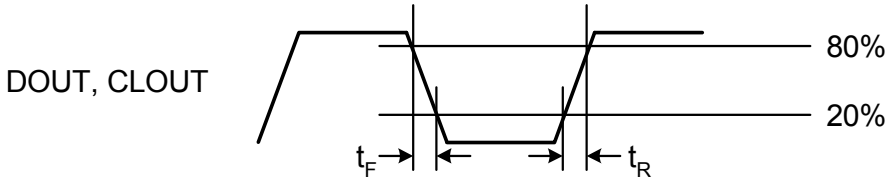



**Figure 2. Rise/Fall Time Characteristics**

## 1.1. Three-Level (3L) Input Pins (No External Resistors)

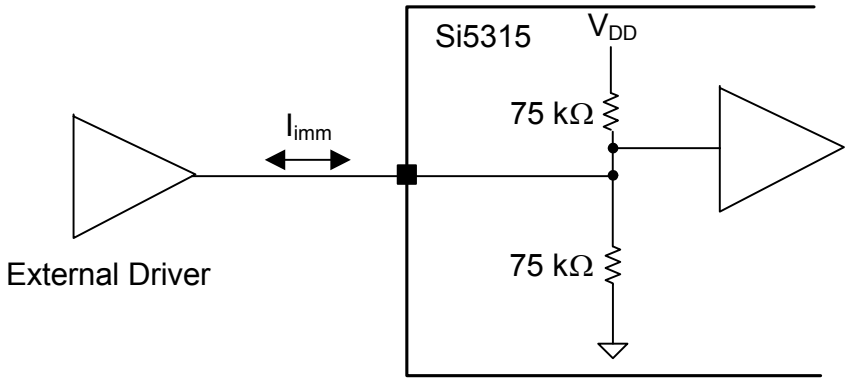
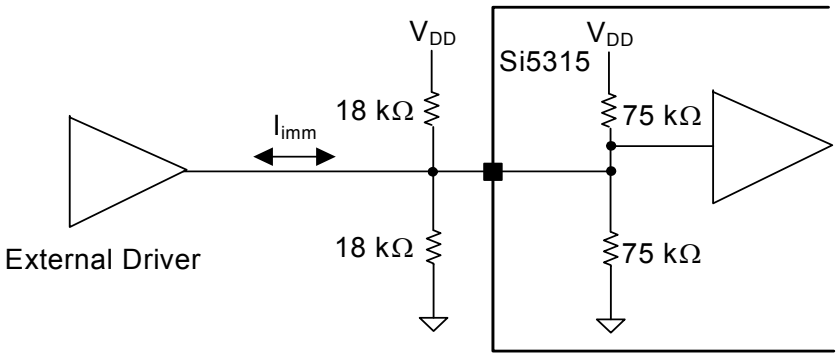



**Figure 3. Three Level Input Pins**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| Input Voltage Low | Vill | — | 0.15 x $V_{DD}$ |
| Input Voltage Mid | Vimm | 0.45 x $V_{DD}$ | 0.55 x $V_{DD}$ |
| Input Voltage High | Vihh | 0.85 x $V_{DD}$ | — |
| Input Low Current | Iill | –6 µA | — |
| Input Mid Current | Iimm | –2 µA | 2 µA |
| Input High Current | Iihh | — | 6 µA |
| **Note:** The above currents are the amount of leakage that the 3L inputs can tolerate from an external driver. | | | |

## 1.2. Three-Level (3L) Input Pins (With External Resistors)




One of eight resistors from a Panasonic EXB-D10C183J
(or similar) resistor pack

**Figure 4. Three Level Input Pins**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| Input Low Current | Iill | –30 µA | — |
| Input Mid Current | Iimm | –11 µA | –11 µA |
| Input High Current | Iihh | — | –30 µA |
| **Note:** The above currents are the amount of leakage that the 3L inputs can tolerate from an external driver. | | | |

- Any resistor pack may be used.
  - The Panasonic EXB-D10C183J is an example.
  - PCB layout is not critical.
- Resistor packs are only needed if the leakage current of the external driver exceeds the listed currents.
- If a pin is tied to ground or $V_{DD}$, no resistors are needed.
- If a pin is left open (no connect), no resistors are needed.

## Table 3. AC Characteristics

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Frequency | $CKN_F$ | Note 1 | 0.008 | — | 644.53 | MHz |
| | | Note 2 | 0.008 | — | 125 | MHz |
| **CKINn Input Pins** | | | | | | |
| Input Duty Cycle (Minimum Pulse Width) | $CKN_{DC}$ | Whichever is smaller[3] | 40 | — | 60 | % |
| | | | 2 | — | — | ns |
| Input Capacitance | $CKN_{CIN}$ | | — | — | 3 | pF |
| Input Rise/Fall Time | $CKN_{TRF}$ | 20–80%<br>See Figure 2 | — | — | 11 | ns |
| **CKOUTn Output Pins** | | | | | | |
| Output Frequency (Output not configured for CMOS or disable) | $CK_{OF}$ | Note 1 | 0.008 | — | 644.53 | MHz |
| | | Note 2 | 0.008 | — | 125 | MHz |
| Maximum Output Frequency in CMOS Format | $CKO_{FMC}$ | | — | — | 125 | MHz |
| Single Ended Output Rise/Fall (20–80%) | $CKO_{TRF}$ | CMOS Output<br>$V_{DD}$ = 1.62<br>Cload = 5 pF | — | — | 8 | ns |
| | | CMOS Output<br>$V_{DD}$ = 2.97<br>Cload = 5 pF | — | — | 2 | ns |
| Output Duty Cycle Differential Uncertainty | $CKO_{DC}$ | 100 Ω Load<br>Line to Line<br>Measured at 50% Point<br>(not for CMOS) | — | — | ±40 | ps |
| **LVCMOS Pins** | | | | | | |
| Input Capacitance | $C_{in}$ | | — | — | 3 | pF |
| CS Deglitch Time | $CKS_{DGT}$ | | — | — | TBD | ns |

**Notes:**

1. Refers to Si5315A speed grade.
2. Refers to Si5315B speed grade.
3. Assumes N3 does not equal 1. IF N3 = 1, $CKN_{DC}$ = 50 µs.

**Table 3. AC Characteristics (Continued)**
($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LVCMOS Output Pins** | | | | | | |
| Rise/Fall Times | $t_{RF}$ | CLOAD = 20 pf<br>See Figure 2 | — | 25 | — | ns |
| LOSn Trigger Window | $LOS_{TRIG}$ | From last CKINn ↑ to internal detection of LOSn | 0.8 x N3 | — | 4.5 x N3 | $T_{CKIN}$ |
| | | Narrowband mode | 250 ns | — | 4.5 x N3 | $T_{CKIN}$ |
| LOSX Trigger Window | $LOSX_{TRIG}$ | From last XA clock ↑ to internal detection of LOSX | 100 | — | 285 | $T_{XA}$ |
| Time to Clear LOS Alarm | $t_{LOSCLR}$ | Measured from appearance of valid CKIN to ↓ of LOS alarm | 90 | — | 220 | ms |
| Time to Declare LOL after LOS | $t_{DECLOL}$ | ↑ LOS to ↑ LOL | — | — | 2 | µs |
| Time to Clear LOL after LOS Cleared | $t_{CLRLOL}$ | ↓ LOS to ↓ LOL | — | — | TBD | ms |
| **PLL Performance** | | | | | | |
| Lock Time | $t_{LOCKHW}$ | ↑ $\overline{RST}$ with valid CKIN to ↓ LOL; BW = 100 Hz | — | | 1.2 | sec |
| Closed Loop Jitter Peaking | $J_{PK}$ | | — | 0.05 | 0.1 | dB |
| Jitter Tolerance | $J_{TOL}$ | | See 3.2.3. "Jitter Tolerance" on page 19. | | | |
| Recovery Time from Disable Mode | $t_{SLP}$ | Exit Disable mode with valid CKIN to ↓ LOL | — | — | TBD | ms |
| Reset to first ↑ on CKOUT | $t_{START}$ | FRQTBL=TBD and Valid, stable clock on CKIN | — | — | 1 | sec |
| Minimum Reset Pulse Width | $t_{RSTMIN}$ | | 1 | — | — | µs |
| Lock Time | $t_{LOCKMP}$ | End of ICAL to ↓ of LOL | — | 35 | 1000 | ms |
| Maximum Frequency Deviation During Self-Calibration | $ICAL_{DF}$ | | –20 | — | 5 | % |
| Power Supply Rejection | PSR | Sine wave noise on $V_{DD}$ to spur at output Differential clock input @ 1.19 Vppd with 0.5 ns rise/fall time (20/80%) $f_{noise}$ = 10 Hz to 10 kHz (non-CMOS Output) | — | — | –100 | dBc/ $mV_{RMS}$ |
| | | $f_{noise}$=10 kHz to 10 MHz | — | — | –75 | dBc/ $mV_{RMS}$ |
| Output Phase Wander with Temperature Gradient | $PH_{DT}$ | Stable input clock Temperature gradient = 10 ºC/min | — | — | TBD | ps/°C/ min |

**Notes:**
1. Refers to Si5315A speed grade.
2. Refers to Si5315B speed grade.
3. Assumes N3 does not equal 1. IF N3 = 1, $CKN_{DC}$ = 50 µs.

**Table 3. AC Characteristics (Continued)**
($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output Clock Initial Phase Step | $t_{P\_STEP}$ | During clock switch CKIN ≥ 19.44 MHz f3 ≥ 128 kHz | — | 100 | 200 | ps |
| | | f3 < 128 kHz | — | 2.2 | — | ns |
| Output Clock Phase Slope | $t_{P\_SLOPE}$ | During clock switch Per GR-CORE-1244 | — | — | 61 | µs/s |
| Holdover Frequency Historical Averaging Time | $t_{HISTAVG}$ | | — | 6.7 | — | sec |
| Holdover Frequency Historical Delay Time | $t_{HISTDEL}$ | | — | 26.2 | — | ms |
| Holdover Initial Frequency Error | $DH_{DFI}$ | External reference clock stable CKIN selected until entering holdover | — | — | 50 | ±ppb |
| | | External resonator stable CKINn selected until entering holdover | — | 50 | — | ±ppb |
| Holdover Frequency Stability vs. Power Supply | $DH_{FVD}$ | External crystal | — | 0.2 | 0.5 | ppm/ 10% Δ in $V_{DD}$ |
| | | External Reference clock | Tracks external reference clock | | | |
| Holdover Frequency Deviation vs. Temperature | $DH_{FVT}$ | External crystal | Tracks external crystal | | | |
| | | External reference clock | Tracks external reference clock | | | |
| Spurious Noise | $SP_{SPUR}$ | Max spur @ n x f3 (n ≥ 1, n x f3 < 100 MHz) | — | — | –75 | dBc |

**Notes:**
1. Refers to Si5315A speed grade.
2. Refers to Si5315B speed grade.
3. Assumes N3 does not equal 1. IF N3 = 1, $CKN_{DC}$ = 50 µs.

**Table 4. Jitter Generation**

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition[1,2,3,4] | | Min | Typ | Max | GR-253 Spec | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Measurement Filter (MHz) | DSPLL BW[1] | | | | | |
| Jitter Gen OC-192 | $J_{GEN}$ | 0.02–80 | 113 Hz[5] | — | TBD | TBD | 30 ps pp/0.3 $UI_{pp}$ | $ps_{PP}$ |
| | | | | — | 0.588 | TBD | N/A | $ps_{rms}$ |
| | | 4–80 | 113 Hz[5] | — | TBD | TBD | 10 ps pp/0.1 $UI_{pp}$ | $ps_{PP}$ |
| | | | | — | 0.513 | TBD | N/A | $ps_{rms}$ |
| | | 0.05–80 | 113 Hz[5] | — | TBD | TBD | 10 ps pp/0.1 $UI_{pp}$ | $ps_{PP}$ |
| | | | | — | 0.569 | TBD | 1.0 $ps_{rms}$ (0.01 $UI_{rms}$ | $ps_{rms}$ |
| Jitter Gen OC-48 | $J_{GEN}$ | 0.012–20 | 113 Hz[5] | — | TBD | TBD | 40.2 ps pp/ (0.1 UIpp) | $ps_{PP}$ |
| | | | | — | 0.551 | TBD | 4.02 $ps_{rms}$ (0.01 $UI_{rms}$ | $ps_{rms}$ |
| | | | 111 Hz[6] | — | TBD | TBD | 40.2 ps pp/ (0.1 UIpp) | $ps_{PP}$ |
| | | | | — | 0.662 | TBD | 4.02 $ps_{rms}$ (0.01 $UI_{rms}$ | $ps_{rms}$ |
| IEEE 802.3 GbE RMS Jitter | $J_{GEN}$ | 1.875–20 | 83 Hz[6] | — | TBD | TBD | N/A | $ps_{PP}$ |
| | | | | — | 0.789 | TBD | N/A | $ps_{rms}$ |

**Notes:**

1. BWSEL [1:0] loop bandwidth settings provided in Table 7 on page 21.
2. 40 MHz fundamental mode crystal used as XA/XB input.
3. $V_{DD}$ = 2.5 V
4. $T_A$ = 85 °C
5. Si5315A test condition: $f_{IN}$ = 19.44 MHz, $f_{OUT}$ = 161.1328125 MHz, LVPECL clock input: 1.19 Vppd with 0.5 ns rise/fall time (20–80%), LVPECL clock output.
6. Si5315B test condition: $f_{IN}$ =19.44 MHz, $f_{OUT}$ = 125 MHz, LVPECL clock input: 1.19 Vppd with 0.5 ns rise/fall time (20-80%), LVPECL clock output.

### Table 5. Thermal Characteristics

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still Air | — | 32 | — | ºC/W |

### Table 6. Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | –0.5 to 3.6 | V |
| LVCMOS Input Voltage | $V_{DIG}$ | –0.3 to ($V_{DD}$ + 0.3) | V |
| Operating Junction Temperature | $T_{JCT}$ | –55 to 150 | C |
| Storage Temperature Range | $T_{STG}$ | –55 to 150 | C |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN– | | 2 | kV |
| ESD MM Tolerance; All pins except CKIN+/CKIN– | | 200 | V |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN– | | 700 | V |
| ESD MM Tolerance; CKIN+/CKIN– | | 150 | V |
| Latch-Up Tolerance | | JESD78 Compliant | |

**Note:** Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

## 2. System Level Overview

The Si5315 provides clock translation, jitter attenuation, and clock distribution for high-performance Synchronous Ethernet line card timing applications. The device accepts two clock inputs ranging from 8 kHz to 644.53 MHz and generates two equal frequency, low jitter clock outputs ranging from 8 kHz to 644.53 MHz. For ease of use, the Si5315 is pin controlled to enable simple device configuration of frequency plans, PLL loop bandwidth, and input clock selection. The DSPLL locks to one of two input reference clocks and provides over 200 frequency translations to synchronize output clocks for Ethernet, SONET/SDH, and PDH line cards. The Si5315 implements internal state machines to control hitless switching between input clocks and holdover. Status alarms, loss of signal (LOS) and loss of lock (LOL) are provided on output pins to indicate a change in device status.

This device is designed for systems with line cards that are synchronized to a redundant, centralized telecom or Ethernet backplane. The Si5315 synchronizes to backplane clocks and generates a multiplied, jitter attenuated Ethernet/SONET/SDH clock or PDH clock. A typical system application is shown in Figure 5. The Si5315 translates a 19.44 MHz clock from the telecom backplane to an Ethernet or SONET/SDH clock frequency to the PHY and filters the jitter to ensure compliance with related ITU-T and Telcordia standards.

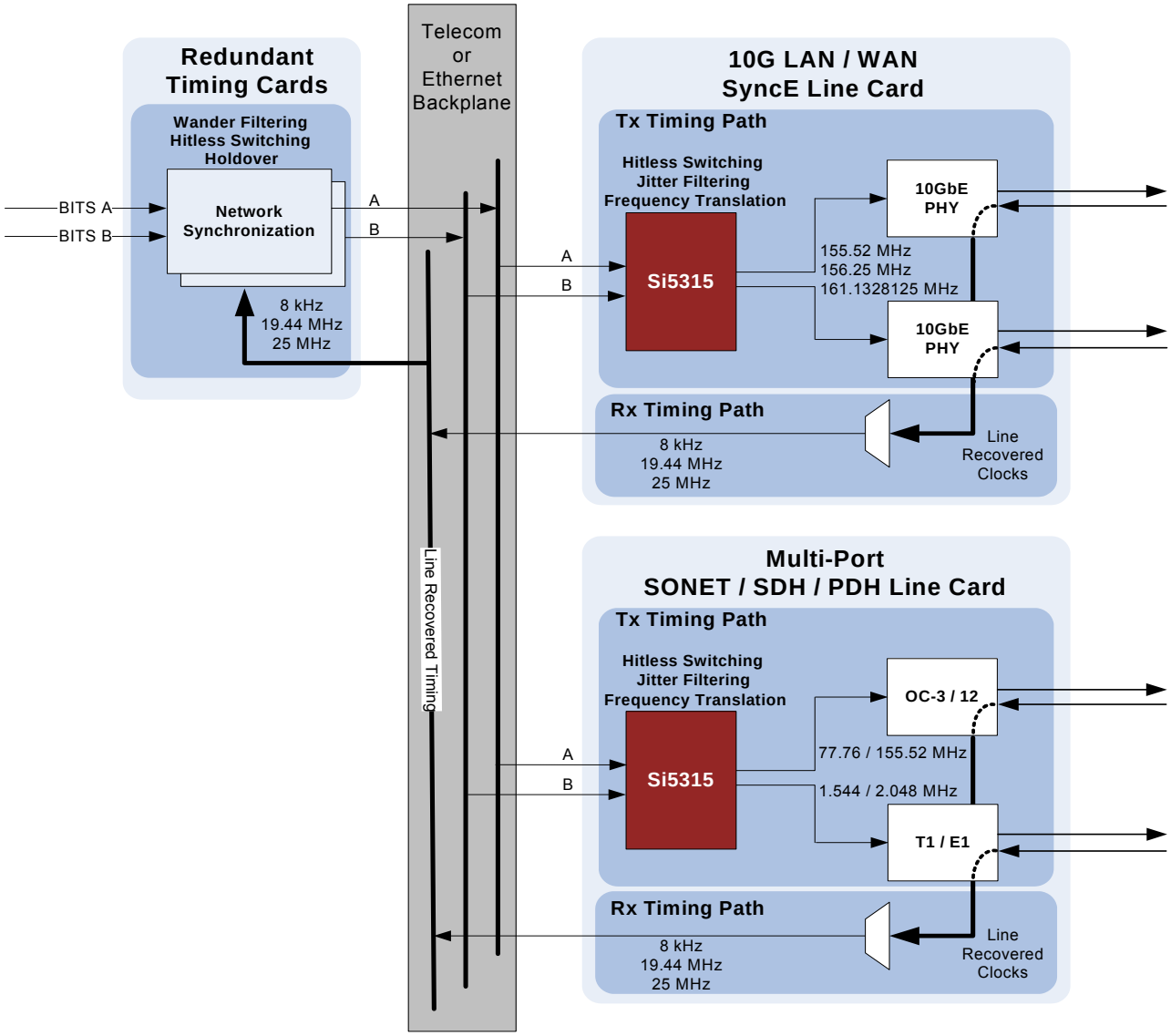



**Figure 5. Typical Si5315 Application**

# 3. Functional Description

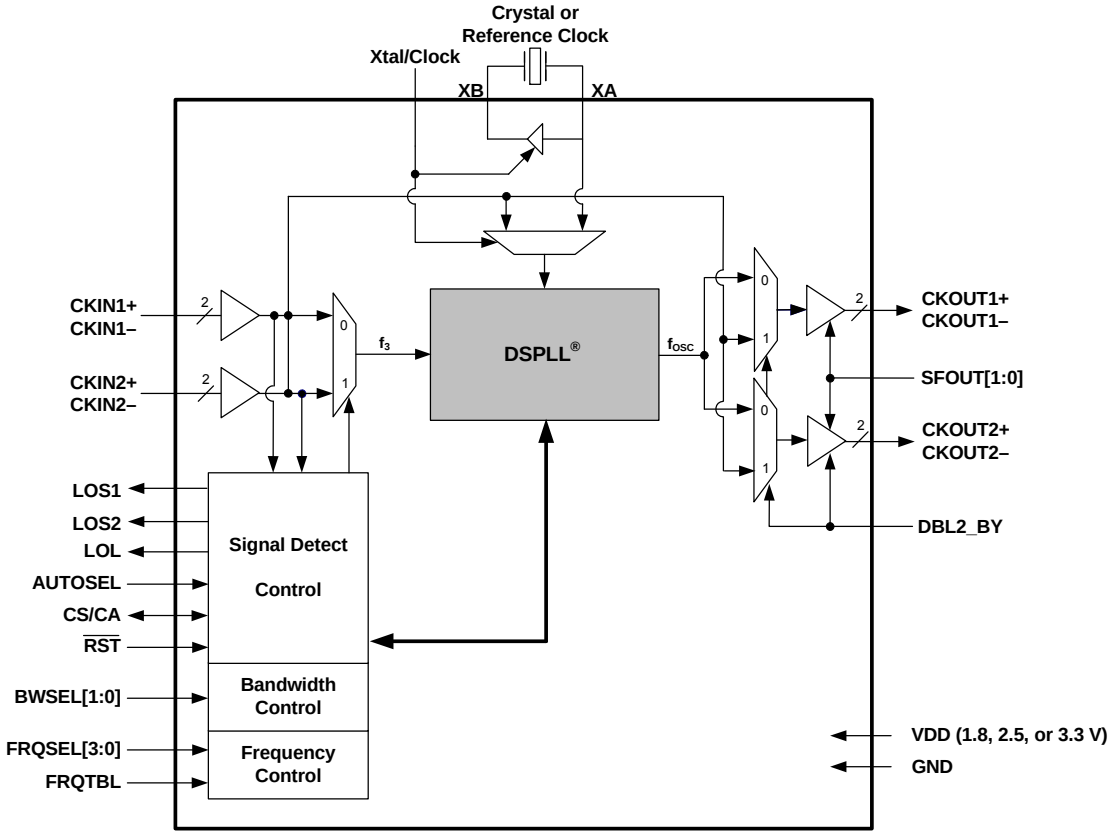



**Figure 6. Detailed Block Diagram**

## 3.1. Overview

The Si5315 is a jitter-attenuating precision clock multiplier for Synchronous Ethernet, SONET/SDH, and PDH (T1/E1) applications. The Si5315 accepts dual clock inputs ranging from 8 kHz to 644.53 MHz and generates two frequency-multiplied clock outputs ranging from 8 kHz to 644.53 MHz. The two input clocks are at the same frequency and the two output clocks are at the same frequency. The input clock frequency and clock multiplication ratio are selectable from a look up table of popular SyncE and T1/E1 rates.

The Si5315 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5315 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 60 to 8.4 kHz.

The Si5315 supports hitless switching between the two input clocks in compliance with ITU-T G.8262 and Telcordia GR-253-CORE and GR-1244-CORE. This feature greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps typ). Manual and automatic revertive and non-revertive input clock switching options are available via the AUTOSEL input pin. The Si5315 monitors both input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. The Si5315 provides a holdover capability that allows the device to continue generation of a stable output clock when the selected input reference is lost.

The Si5315 has two differential clock outputs. The signal format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. The second clock output can be powered down to minimize power consumption. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device operates from a single 1.8, 2.5, or 3.3 V supply.

## 3.2. PLL Performance

The Si5315 provides extremely low jitter generation, a well-controlled jitter transfer function, and high jitter tolerance due to the high level of integration.

### 3.2.1. Jitter Generation

Jitter generation is defined as the amount of jitter produced at the output of the device with a jitter free input clock. Generated jitter arises from sources within the VCO and other PLL components. Jitter generation is a function of the PLL bandwidth setting. Higher loop bandwidth settings may result in lower jitter generation, but may result in less attenuation of jitter that might be present on the input clock signal.

### 3.2.2. Jitter Transfer

Jitter transfer is defined as the ratio of output signal jitter to input signal jitter for a specified jitter frequency. The jitter transfer characteristic determines the amount of input clock jitter that passes to the outputs. The DSPLL technology used in the Si5315 provides tightly controlled jitter transfer curves because the PLL gain parameters are determined largely by digital circuits which do not vary over supply voltage, process, and temperature. In a system application, a well-controlled transfer curve minimizes the output clock jitter variation from board to board and provides more consistent system level jitter performance.

The jitter transfer characteristic is a function of the loop bandwidth setting. Lower bandwidth settings result in more jitter attenuation of the incoming clock, but may result in higher jitter generation. Figure 7 shows the jitter transfer curve mask.

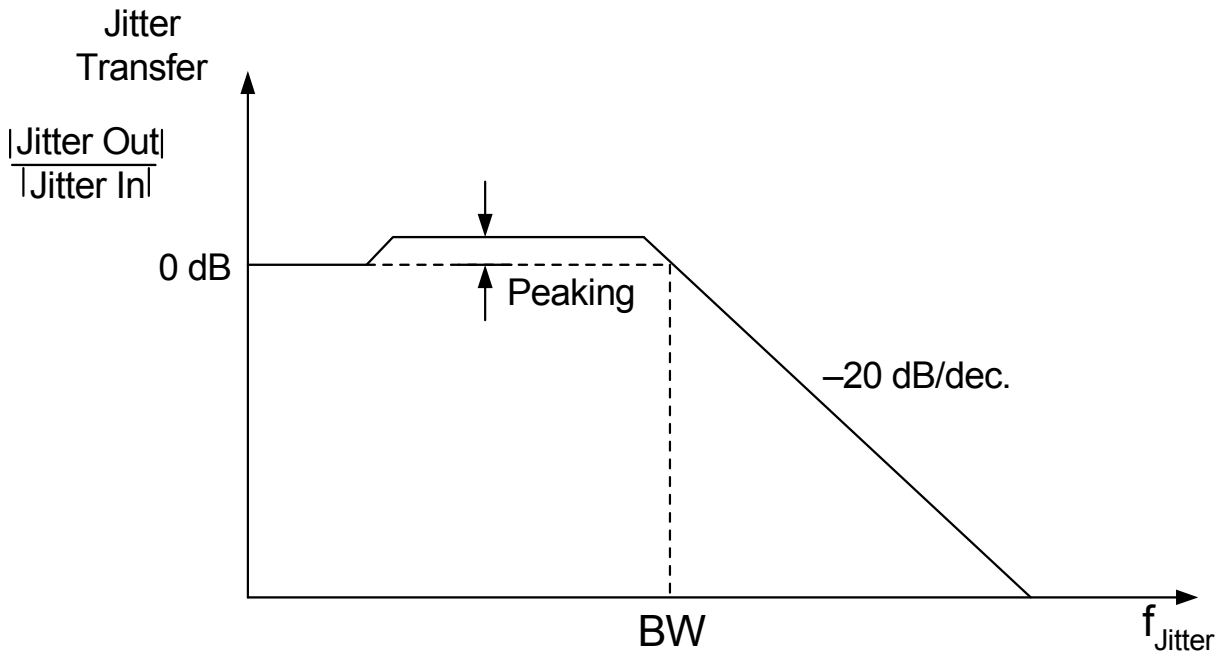



**Figure 7. PLL Jitter Transfer Mask/Template**

### 3.2.3. Jitter Tolerance

Jitter tolerance is defined as the maximum peak-to-peak sinusoidal jitter that can be present on the incoming clock before the DSPLL loses lock. The tolerance is a function of the jitter frequency, because tolerance improves for lower input jitter frequency.

The jitter tolerance of the DSPLL is a function of the loop bandwidth setting. Figure 8 shows the general shape of the jitter tolerance curve versus input jitter frequency. For jitter frequencies above the loop bandwidth, the tolerance is a constant value $A_{j0}$. Beginning at the PLL bandwidth, the tolerance increases at a rate of 20 dB/decade for lower input jitter frequencies.

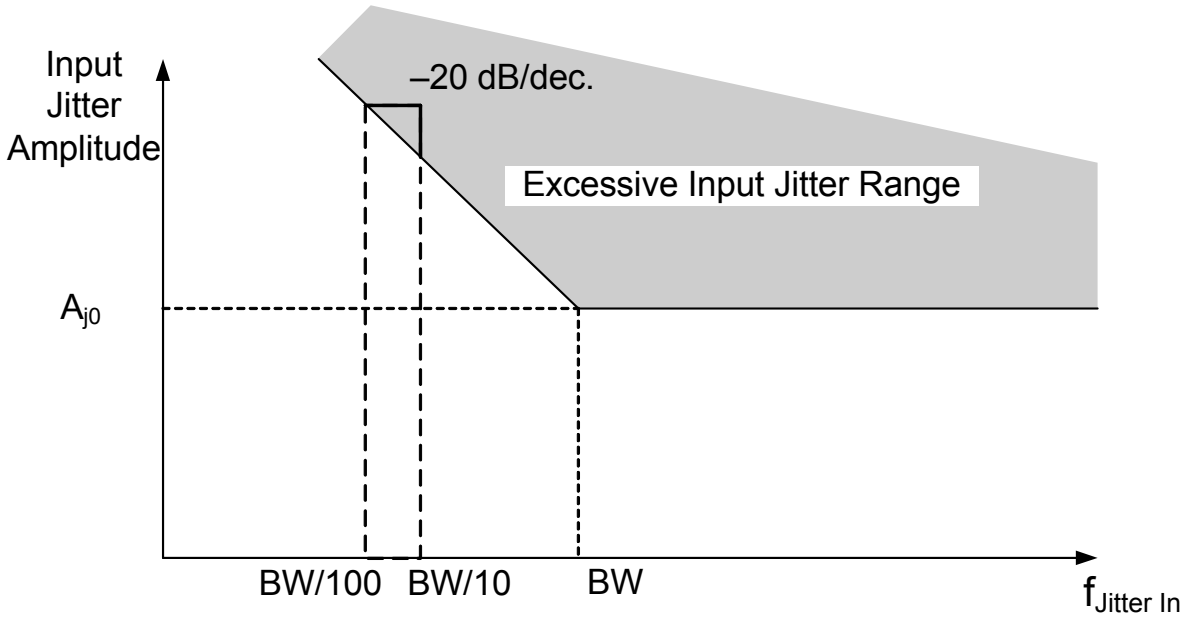



**Figure 8. Jitter Tolerance Mask/Template**

The equation for the high frequency jitter tolerance can be expressed as a function of the PLL loop bandwidth (i.e., BW):

$$A_{j0} = \frac{5000}{BW} \text{ ns pk-pk}$$

For example, the jitter tolerance when $f_{in}$ = 19.44 MHz, $f_{out}$ = 161.13 MHz and the loop bandwidth (BW) is 113 Hz:

$$A_{j0} = \frac{5000}{113} = 44.24 \text{ ns pk-pk}$$

### 3.2.4. Jitter Attenuation Performance

The Internal VCO uses the reference clock on the XA/XB pins as its reference for jitter attenuation. The XA/XB pins support either a crystal input or an input buffer single-ended or differential clock input, such that an external oscillator can become the reference source. In either case, the device accepts a wide margin in absolute frequency of the reference input. (See 4.5. "Holdover Mode" on page 35.) In holdover, the Si5315's output clock stability matches the reference supplied on the XA/XB pins. The external crystal or reference clock must be selected based on the stability requirements of the application if holdover is a key requirement.

However, care must be exercised in certain areas for optimum performance. For examples of connections to the XA/XB pins, refer to 6. "Crystal/Reference Clock Input" on page 41.

# 4. Frequency Plan Tables

For ease of use, the Si5315 is pin controlled to enable simple device configuration of the frequency plan and PLL loop bandwidth via a predefined look up table. The DSPLL has been optimized for each frequency multiplication and PLL loop bandwidth provided in Table 7 on page 21.

Many of the control inputs are three levels: High, Low, and Medium. High and Low are standard voltage levels determined by the supply voltage: $V_{DD}$ and Ground. If the input pin is left floating, it is driven to nominally half of $V_{DD}$. Effectively, this creates three logic levels for these controls. See sections 7. "Power Supply Filtering" on page 44 and 1.2. "Three-Level (3L) Input Pins (With External Resistors)" on page 10 for additional information.

## 4.1. Frequency Multiplication Plan

The input to output clock multiplication is set by the 3-level FRQSEL[3:0] pins. The device provides a wide range of commonly used SyncE, SONET/SDH, and PDH frequency translations. The CKIN1 and CKIN2 inputs must be the same frequency as specified in Table 7. Both CKOUT1 and CKOUT2 outputs are at the same frequency.

### 4.1.1. PLL Loop Bandwidth Plan

The Si5315's loop bandwidth ranges from 60 Hz to 8.4 kHz. For each frequency multiplication, its corresponding loop bandwidth is provided in a simple look up table. (See Table 7 on page 21.) The loop bandwidth (BW) is digitally programmable using the 3-level BWSEL [1:0] and FRQTBL input pins.

## Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 1 | 0.008 | 0.008 | L | LLLL | 257 | 60 | — | — | — | — | — |
| 2 | 0.008 | 1.544 | L | LLLM | 257 | 60 | — | — | — | — | — |
| 3 | 0.008 | 2.048 | L | LLLH | 257 | 60 | — | — | — | — | — |
| 4 | 0.008 | 8.192 | L | LLML | 257 | 60 | — | — | — | — | — |
| 5 | 0.008 | 19.44 | L | LLMM | 257 | 60 | — | — | — | — | — |
| 6 | 0.008 | 25 | L | LLMH | 257 | 60 | — | — | — | — | — |
| 7 | 0.008 | 32.768 | L | LLHL | 257 | 60 | — | — | — | — | — |
| 8 | 0.008 | 34.368 | M | LLLL | 257 | 60 | — | — | — | — | — |
| 9 | 0.008 | 38.88 | M | LLLM | 257 | 60 | — | — | — | — | — |
| 10 | 0.008 | 44.736 | M | LLLH | 257 | 60 | — | — | — | — | — |
| 11 | 0.008 | 51.84 | M | LLML | 257 | 60 | — | — | — | — | — |
| 12 | 0.008 | 65.536 | M | LLMM | 257 | — | — | — | — | — | — |
| 13 | 0.008 | 77.76 | M | LLMH | 257 | 60 | — | — | — | — | — |
| 14 | 0.008 | 125 | M | LLHL | 257 | 60 | — | — | — | — | — |
| 15 | 0.008 | 155.52 | H | LLLL | 257 | 60 | — | — | — | — | — |
| 16 | 0.008 | 156.25 | H | LLLM | 257 | 60 | — | — | — | — | — |
| 17 | 0.008 | 311.04 | H | LLLH | 257 | 60 | — | — | — | — | — |
| 18 | 0.008 | 312.5 | H | LLML | 257 | 60 | — | — | — | — | — |
| 19 | 0.008 | 622.08 | H | LLMM | 257 | 60 | — | — | — | — | — |
| 20 | 1.544 | 0.008 | L | LLHM | 257 | 60 | — | — | — | — | — |
| 21 | 1.544 | 1.544 | L | LLHH | — | — | 6047 | 1451 | 359 | 179 | 89 |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 22 | 1.544 | 2.048 | L | LMLL | 257 | 60 | — | — | — | — | — |
| 23 | 1.544 | 8.192 | L | LMLM | 257 | 60 | — | — | — | — | — |
| 24 | 1.544 | 19.44 | L | LMLH | 257 | 60 | — | — | — | — | — |
| 25 | 1.544 | 25 | L | LMML | 257 | 60 | — | — | — | — | — |
| 26 | 1.544 | 32.768 | L | LMMM | 257 | 60 | — | — | — | — | — |
| 27 | 1.544 | 34.368 | M | LLHM | 257 | 60 | — | — | — | — | — |
| 28 | 1.544 | 38.88 | M | LLHH | 257 | 60 | — | — | — | — | — |
| 29 | 1.544 | 44.736 | M | LMLL | 257 | 60 | — | — | — | — | — |
| 30 | 1.544 | 51.84 | M | LMLM | 257 | 60 | — | — | — | — | — |
| 31 | 1.544 | 65.536 | M | LMLH | 257 | — | — | — | — | — | — |
| 32 | 1.544 | 77.76 | M | LMML | 257 | 60 | — | — | — | — | — |
| 33 | 1.544 | 125 | M | LMMM | 257 | 60 | — | — | — | — | — |
| 34 | 1.544 | 155.52 | H | LLMH | 257 | 60 | — | — | — | — | — |
| 35 | 1.544 | 156.25 | H | LLHL | 257 | 60 | — | — | — | — | — |
| 36 | 1.544 | 311.04 | H | LLHM | 257 | 60 | — | — | — | — | — |
| 37 | 1.544 | 312.5 | H | LLHH | 257 | 60 | — | — | — | — | — |
| 38 | 1.544 | 622.08 | H | LMLL | 257 | 60 | — | — | — | — | — |
| 39 | 2.048 | 0.008 | L | LMMH | 2089 | 485 | 240 | 59 | — | — | — |
| 40 | 2.048 | 1.544 | L | LMHL | 1037 | 242 | 119 | — | — | — | — |
| 41 | 2.048 | 2.048 | L | LMHM | — | — | 3949 | 959 | 238 | 118 | 59 |
| 42 | 2.048 | 8.192 | L | LMHH | — | — | 3949 | 959 | 238 | 118 | 59 |
| 43 | 2.048 | 19.44 | L | LHLL | — | — | 3946 | 958 | 238 | 118 | 59 |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 44 | 2.048 | 25 | L | LHLM | 2087 | 485 | 240 | — | — | — | — |
| 45 | 2.048 | 32.768 | L | LHLH | — | — | 3947 | 959 | 238 | 118 | 59 |
| 46 | 2.048 | 34.368 | M | LMMH | — | 8163 | 3935 | 958 | 238 | 118 | — |
| 47 | 2.048 | 38.88 | M | LMHL | — | — | 3946 | 958 | 238 | 118 | 59 |
| 48 | 2.048 | 44.736 | M | LMHM | — | 3983 | 1944 | 477 | 118 | 59 | — |
| 49 | 2.048 | 51.84 | M | LMHH | — | — | 3946 | 958 | 238 | 118 | 59 |
| 50 | 2.048 | 65.536 | M | LHLL | — | 8185 | 3940 | 958 | 238 | 118 | — |
| 51 | 2.048 | 77.76 | M | LHLM | — | — | 3946 | 958 | 238 | 118 | 59 |
| 52 | 2.048 | 125 | M | LHLH | 1037 | 242 | 119 | — | — | — | — |
| 53 | 2.048 | 155.52 | H | LMLM | — | — | 3946 | 958 | 238 | 118 | 59 |
| 54 | 2.048 | 156.25 | H | LMLH | 1037 | 242 | 119 | — | — | — | — |
| 55 | 2.048 | 311.04 | H | LMML | — | — | 3946 | 958 | 238 | 118 | 59 |
| 56 | 2.048 | 312.5 | H | LMMM | 1037 | 242 | 119 | — | — | — | — |
| 57 | 2.048 | 622.08 | H | LMMH | — | — | 3946 | 958 | 238 | 118 | 59 |
| 58 | 8.192 | 0.008 | L | LHML | 2089 | 485 | 240 | 59 | — | — | — |
| 59 | 8.192 | 1.544 | L | LHMM | 1037 | 242 | 119 | — | — | — | — |
| 60 | 8.192 | 2.048 | L | LHMH | — | — | 6434 | 1541 | 381 | 190 | 95 |
| 61 | 8.192 | 8.192 | L | LHHL | — | — | 6434 | 1541 | 381 | 190 | 95 |
| 62 | 8.192 | 19.44 | L | LHHM | — | — | 3946 | 958 | 238 | 118 | 59 |
| 63 | 8.192 | 25 | L | LHHH | 2087 | 485 | 240 | — | — | — | — |
| 64 | 8.192 | 32.768 | L | MLLL | — | — | 6431 | 1541 | 381 | 190 | 95 |
| 65 | 8.192 | 34.368 | M | LHML | — | 8163 | 3935 | 958 | 238 | 118 | — |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 66 | 8.192 | 38.88 | M | LHMM | — | — | 3946 | 958 | 238 | 118 | 59 |
| 67 | 8.192 | 44.736 | M | LHMH | — | 3983 | 1944 | 477 | 118 | 59 | — |
| 68 | 8.192 | 51.84 | M | LHHL | — | — | 3946 | 958 | 238 | 118 | 59 |
| 69 | 8.192 | 65.536 | M | LHHM | — | — | 6411 | 1539 | 381 | 190 | 95 |
| 70 | 8.192 | 77.76 | M | LHHH | — | — | 3946 | 958 | 238 | 118 | 59 |
| 71 | 8.192 | 125 | M | MLLL | 1037 | 242 | 119 | — | — | — | — |
| 72 | 19.44 | 0.008 | L | MLLM | 1759 | 409 | 202 | — | — | — | — |
| 73 | 19.44 | 1.544 | L | MLLH | — | 2779 | 1362 | 335 | 83 | — | — |
| 74 | 19.44 | 2.048 | L | MLML | — | 3348 | 1638 | 402 | 100 | — | — |
| 75 | 19.44 | 8.192 | L | MLMM | — | 3348 | 1638 | 402 | 100 | — | — |
| 76 | 19.44 | 19.44 | L | MLMH | — | — | 7706 | 1832 | 452 | 225 | 112 |
| 77 | 19.44 | 25 | L | MLHL | — | 2778 | 1362 | 335 | 83 | — | — |
| 78 | 19.44 | 32.768 | L | MLHM | — | — | 5022 | 1215 | 301 | 150 | 75 |
| 79 | 19.44 | 34.368 | M | MLLM | — | 5662 | 2749 | 672 | 167 | 83 | — |
| 80 | 19.44 | 38.88 | M | MLLH | — | — | 7703 | 1832 | 452 | 225 | 112 |
| 81 | 19.44 | 44.736 | M | MLML | — | 5653 | 2747 | 672 | 167 | 83 | — |
| 82 | 19.44 | 51.84 | M | MLMM | — | — | 7696 | 1832 | 452 | 225 | 112 |
| 83 | 19.44 | 65.536 | M | MLMH | 2618 | 607 | 300 | 74 | — | — | — |
| 84 | 19.44 | 77.76 | M | MLHL | — | — | 7696 | 1832 | 452 | 225 | 112 |
| 85 | 19.44 | 125 | M | MLHM | 3960 | 913 | 450 | 111 | — | — | — |
| 86 | 19.44 | 155.52 | H | LMHL | — | — | 7696 | 1832 | 452 | 225 | 112 |
| 87 | 19.44 | 156.25 | H | LMHM | 6003 | 1373 | 677 | 167 | — | — | — |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 88 | 19.44 | 161.1328 | H | LMHH | 484 | 113 | — | — | — | — | — |
| 89 | 19.44 | 311.04 | H | LHLL | — | — | 7696 | 1832 | 452 | 225 | 112 |
| 90 | 19.44 | 312.5 | H | LHLM | 6003 | 1373 | 677 | 167 | — | — | — |
| 91 | 19.44 | 622.08 | H | LHLH | — | — | 7696 | 1832 | 452 | 225 | 112 |
| 92 | 19.44 | 644.5313 | H | LHML | 103 | — | — | — | — | — | — |
| 93 | 25 | 0.008 | L | MLHH | — | — | 7045 | 1681 | 415 | 207 | 103 |
| 94 | 25 | 1.544 | L | MMLL | 6741 | 1529 | 753 | 186 | — | — | — |
| 95 | 25 | 2.048 | L | MMLM | 1299 | 303 | 150 | — | — | — | — |
| 96 | 25 | 8.192 | L | MMLH | 6737 | 1529 | 753 | 186 | — | — | — |
| 97 | 25 | 19.44 | L | MMML | — | — | 6551 | 1568 | 387 | 193 | 96 |
| 98 | 25 | 25 | L | MMMM | — | — | 7615 | 1812 | 447 | 223 | 111 |
| 99 | 25 | 32.768 | L | MMMH | 6737 | 1529 | 753 | 186 | — | — | — |
| 100 | 25 | 34.368 | M | MLHH | 6722 | 1528 | 753 | 186 | — | — | — |
| 101 | 25 | 38.88 | M | MMLL | 6729 | 1529 | 753 | 186 | — | — | — |
| 102 | 25 | 44.736 | M | MMLM | 1298 | 303 | 150 | — | — | — | — |
| 103 | 25 | 51.84 | M | MMLH | — | 7988 | 3846 | 936 | 232 | 116 | — |
| 104 | 25 | 65.536 | M | MMML | 1298 | 303 | 150 | — | — | — | — |
| 105 | 25 | 77.76 | M | MMMM | 6706 | 1528 | 753 | 186 | — | — | — |
| 106 | 25 | 125 | M | MMMH | — | — | 7606 | 1811 | 447 | 223 | 111 |
| 107 | 25 | 155.52 | H | LHMM | 1298 | 303 | 150 | — | — | — | — |
| 108 | 25 | 156.25 | H | LHMH | — | — | 7606 | 1811 | 447 | 223 | 111 |
| 109 | 25 | 161.1328 | H | LHHL | — | — | 6106 | 1468 | 363 | 181 | 90 |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 110 | 25 | 311.04 | H | LHHM | 1298 | 303 | 150 | — | — | — | — |
| 111 | 25 | 312.5 | H | LHHH | — | — | 7606 | 1811 | 447 | 223 | 111 |
| 112 | 25 | 622.08 | H | MLLL | 1298 | 303 | 150 | — | — | — | — |
| 113 | 25 | 644.5313 | H | MLLM | — | — | 6106 | 1468 | 363 | 181 | 90 |
| 114 | 32.768 | 0.008 | L | MMHL | 2089 | 485 | 240 | 59 | — | — | — |
| 115 | 32.768 | 1.544 | L | MMHM | 1037 | 242 | 119 | — | — | — | — |
| 116 | 32.768 | 2.048 | L | MMHH | — | — | 7187 | 1714 | 423 | 211 | 105 |
| 117 | 32.768 | 8.192 | L | MHLL | — | — | 7632 | 1816 | 448 | 223 | 111 |
| 118 | 32.768 | 19.44 | L | MHLM | — | — | 3946 | 958 | 238 | 118 | 59 |
| 119 | 32.768 | 25 | L | MHLH | 2087 | 485 | 240 | — | — | — | — |
| 120 | 32.768 | 32.768 | L | MHML | — | — | 7632 | 1816 | 448 | 223 | 111 |
| 121 | 32.768 | 34.368 | M | MMHL | — | 8163 | 3935 | 958 | 238 | 118 | — |
| 122 | 32.768 | 38.88 | M | MMHM | — | — | — | 958 | 238 | 118 | 59 |
| 123 | 32.768 | 44.736 | M | MMHH | — | 3983 | 1944 | 477 | 118 | 59 | — |
| 124 | 32.768 | 51.84 | M | MHLL | — | — | 3946 | 958 | 238 | 118 | 59 |
| 125 | 32.768 | 65.536 | M | MHLM | — | — | 7604 | 1815 | 448 | 223 | 111 |
| 126 | 32.768 | 77.76 | M | MHLH | — | — | 3946 | 958 | 238 | 118 | 59 |
| 127 | 32.768 | 125 | M | MHML | 1037 | 242 | 119 | — | — | — | — |
| 128 | 77.76 | 0.008 | L | MHMM | 2089 | 485 | 240 | 59 | — | — | — |
| 129 | 77.76 | 1.544 | L | MHMH | — | 2779 | 1362 | 335 | 83 | — | — |
| 130 | 77.76 | 2.048 | L | MHHL | — | — | 6804 | 1626 | 402 | 200 | 100 |
| 131 | 77.76 | 19.44 | L | MHHM | — | — | 7905 | 1879 | 464 | 231 | 115 |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

## Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 132 | 77.76 | 25 | L | MHHH | — | 2778 | 1362 | 335 | 83 | — | — |
| 133 | 77.76 | 34.368 | M | MHMM | — | — | 6798 | 1626 | 402 | 200 | 100 |
| 134 | 77.76 | 38.88 | M | MHMH | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 135 | 77.76 | 44.736 | M | MHHL | — | — | 6756 | 1623 | 402 | 200 | 100 |
| 136 | 77.76 | 51.84 | M | MHHM | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 137 | 77.76 | 65.536 | M | MHHH | — | 2461 | 1208 | 298 | 74 | — | — |
| 138 | 77.76 | 77.76 | M | HLLL | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 139 | 77.76 | 125 | M | HLLM | 5336 | 1220 | 602 | 148 | — | — | — |
| 140 | 77.76 | 155.52 | H | MLLH | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 141 | 77.76 | 156.25 | H | MLML | 6003 | 1373 | 677 | 167 | — | — | — |
| 142 | 77.76 | 161.1328 | H | MLMM | 484 | 113 | — | — | — | — | — |
| 143 | 77.76 | 311.04 | H | MLMH | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 144 | 77.76 | 312.5 | H | MLHL | 6003 | 1373 | 677 | 167 | — | — | — |
| 145 | 77.76 | 622.08 | H | MLHM | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 146 | 77.76 | 644.5313 | H | MLHH | 484 | 113 | — | — | — | — | — |
| 147 | 125 | 0.008 | L | HLLL | — | — | 7045 | 1681 | 415 | 207 | 103 |
| 148 | 125 | 1.544 | L | HLLM | 6741 | 1529 | 753 | 186 | — | — | — |
| 149 | 125 | 2.048 | L | HLLH | 1299 | 303 | 150 | — | — | — | — |
| 150 | 125 | 19.44 | L | HLML | — | — | 6551 | 1568 | 387 | 193 | 96 |
| 151 | 125 | 25 | L | HLMM | — | — | 7862 | 1870 | 462 | 230 | 115 |
| 152 | 125 | 34.368 | M | HLLH | 6722 | 1528 | 753 | 186 | — | — | — |
| 153 | 125 | 38.88 | M | HLML | 6729 | 1529 | 753 | 186 | — | — | — |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 154 | 125 | 44.736 | M | HLMM | 1298 | 303 | 150 | — | — | — | — |
| 155 | 125 | 51.84 | M | HLMH | — | 7988 | 3846 | 936 | 232 | 116 | — |
| 156 | 125 | 65.536 | M | HLHL | 1298 | 303 | 150 | — | — | — | — |
| 157 | 125 | 77.76 | M | HLHM | 6706 | 1528 | 753 | 186 | — | — | — |
| 158 | 125 | 125 | M | HLHH | — | — | 7862 | 1870 | 462 | 230 | 115 |
| 159 | 125 | 155.52 | H | MMLL | 1298 | 303 | 150 | — | — | — | — |
| 160 | 125 | 156.25 | H | MMLM | — | — | 7862 | 1870 | 462 | 230 | 115 |
| 161 | 125 | 161.1328 | H | MMLH | — | — | 7718 | 1839 | 454 | 226 | 113 |
| 162 | 125 | 311.04 | H | MMML | 1298 | 303 | 150 | — | — | — | — |
| 163 | 125 | 312.5 | H | MMMM | — | — | 7862 | 1870 | 462 | 230 | 115 |
| 164 | 125 | 622.08 | H | MMMH | 1298 | 303 | 150 | — | — | — | — |
| 165 | 125 | 644.5313 | H | MMHL | — | — | 7718 | 1839 | 454 | 226 | 113 |
| 166 | 155.52 | 0.008 | L | HLMH | 2089 | 485 | 240 | 59 | — | — | — |
| 167 | 155.52 | 1.544 | L | HLHL | — | 2779 | 1362 | 335 | 83 | — | — |
| 168 | 155.52 | 2.048 | L | HLHM | — | — | 7606 | 1809 | 447 | 223 | 111 |
| 169 | 155.52 | 19.44 | L | HLHH | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 170 | 155.52 | 25 | L | HMLL | — | 2778 | 1362 | 335 | 83 | — | — |
| 171 | 155.52 | 77.76 | H | MMHM | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 172 | 155.52 | 125 | H | MMHH | 5336 | 1220 | 602 | 148 | — | — | — |
| 173 | 155.52 | 155.52 | H | MHLL | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 174 | 155.52 | 156.25 | H | MHLM | 6003 | 1373 | 677 | 167 | — | — | — |
| 175 | 155.52 | 161.1328 | H | MHLH | 484 | 113 | — | — | — | — | — |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 176 | 155.52 | 311.04 | H | MHML | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 177 | 155.52 | 312.5 | H | MHMM | 6003 | 1373 | 677 | 167 | — | — | — |
| 178 | 155.52 | 622.08 | H | MHMH | — | — | 7905 | 1879 | 464 | 231 | 115 |
| 179 | 155.52 | 644.5313 | H | MHHL | 828 | 193 | 95 | — | — | — | — |
| 180 | 156.25 | 0.008 | L | HMLM | — | — | 6123 | 1469 | 363 | 181 | 90 |
| 181 | 156.25 | 1.544 | L | HMLH | 1627 | 379 | 187 | — | — | — | — |
| 182 | 156.25 | 2.048 | L | HMML | 322 | 75 | — | — | — | — | — |
| 183 | 156.25 | 19.44 | L | HMMM | — | — | 4852 | 1172 | 290 | 145 | 72 |
| 184 | 156.25 | 25 | L | HMMH | — | — | 7835 | 1864 | 460 | 229 | 114 |
| 185 | 156.25 | 77.76 | H | MHHM | 1625 | 379 | 187 | — | — | — | — |
| 186 | 156.25 | 125 | H | MHHH | — | — | 7835 | 1864 | 460 | 229 | 114 |
| 187 | 156.25 | 155.52 | H | HLLL | 322 | 75 | — | — | — | — | — |
| 188 | 156.25 | 156.25 | H | HLLM | — | — | 7835 | 1864 | 460 | 229 | 114 |
| 189 | 156.25 | 161.1328 | H | HLLH | — | — | 7718 | 1839 | 454 | 226 | 113 |
| 190 | 156.25 | 311.04 | H | HLML | 322 | 75 | — | — | — | — | — |
| 191 | 156.25 | 312.5 | H | HLMM | — | — | 7835 | 1864 | 460 | 229 | 114 |
| 192 | 156.25 | 622.08 | H | HLMH | 322 | 75 | — | — | — | — | — |
| 193 | 156.25 | 644.5313 | H | HLHL | — | — | 7718 | 1839 | 454 | 226 | 113 |
| 194 | 161.1328 | 0.008 | L | HMHL | 225 | — | — | — | — | — | — |
| 195 | 161.1328 | 1.544 | L | HMHM | 151 | — | — | — | — | — | — |
| 196 | 161.1328 | 2.048 | L | HMHH | 225 | — | — | — | — | — | — |
| 197 | 161.1328 | 19.44 | L | HHLL | 679 | 159 | 78 | — | — | — | — |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

**Table 7. Look Up Tables for Clock Multiplication and Loop Bandwidth Settings (Continued)**

| Plan # | $f_{IN}$ (MHz) | $f_{OUT}$ (MHz) | FRQTBL | FRQSEL [3:0] | Loop Bandwidth Selection (Hz), BWSEL[1:0] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LM | LH | ML | MM | MH | HL | HH |
| 198 | 161.1328 | 25 | L | HHLM | 678 | 159 | 78 | — | — | — | — |
| 199 | 161.1328 | 77.76 | H | HLHM | 678 | 159 | 78 | — | — | — | — |
| 200 | 161.1328 | 125 | H | HLHH | — | — | 7179 | 1721 | 426 | 212 | 106 |
| 201 | 161.1328 | 156.25 | H | HMLL | — | — | 7019 | 1683 | 416 | 207 | 103 |
| 202 | 161.1328 | 161.1328 | H | HMLM | 332 | 78 | — | — | — | — | — |
| 203 | 161.1328 | 311.04 | H | HMLH | — | — | 6381 | 1530 | 378 | 189 | 94 |
| 204 | 161.1328 | 312.5 | H | HMML | 3873 | 892 | 440 | 109 | — | — | — |
| 205 | 161.1328 | 644.5313 | H | HMMM | 151 | — | — | — | — | — | — |
| 206 | 644.5313 | 0.008 | L | HHLH | 880 | 206 | 101 | — | — | — | — |
| 207 | 644.5313 | 1.544 | L | HHML | 413 | 96 | — | — | — | — | — |
| 208 | 644.5313 | 2.048 | L | HHMM | — | 3373 | 1650 | 405 | 101 | — | — |
| 209 | 644.5313 | 19.44 | L | HHMH | — | 3641 | 1779 | 437 | 108 | — | — |
| 210 | 644.5313 | 25 | L | HHHL | — | — | 7886 | 1875 | 463 | 231 | 115 |
| 211 | 644.5313 | 77.76 | H | HMMH | 828 | 193 | 95 | — | — | — | — |
| 212 | 644.5313 | 125 | H | HMHL | — | — | 7732 | 1840 | 454 | 226 | 113 |
| 213 | 644.5313 | 155.52 | H | HMHM | 828 | 193 | 95 | — | — | — | — |
| 214 | 644.5313 | 156.25 | H | HMHH | — | — | 7732 | 1840 | 454 | 226 | 113 |
| 215 | 644.5313 | 161.1328 | H | HHLL | — | — | 7895 | 1880 | 464 | 231 | 115 |
| 216 | 644.5313 | 311.04 | H | HHLM | 828 | 193 | 95 | — | — | — | — |
| 217 | 644.5313 | 312.5 | H | HHLH | 206 | — | — | — | — | — | — |
| 218 | 644.5313 | 622.08 | H | HHML | 120 | — | — | — | — | — | — |
| 219 | 644.5313 | 644.5313 | H | HHMM | — | — | 7895 | 1880 | 464 | 231 | 115 |

**Notes:**

1. $F_{IN}$ and $F_{OUT}$ frequency values may be rounded off. For exact multiplication ratios, please contact Silicon Labs.
2. Si5315A supports all frequency plans. FRQTBL = L/H/M applies for normal operation.
3. Si5315B supports frequency plans up to 125 MHz. FRQTBL = H is reserved. L/M are used for normal operation.

## 4.2. PLL Self-Calibration

An internal self-calibration (ICAL) is performed before operation to optimize loop parameters and jitter performance. While the self-calibration is being performed, the DSPLL is being internally controlled by the self-calibration state machine. The LOL alarm will be active during ICAL. The self-calibration time $t_{LOCKHW}$ is given in Table 3, “AC Characteristics”.

Any of the following events will trigger a self-calibration:

- Power-on-reset (POR)
- Release of the external reset pin $\overline{RST}$ (transition of $\overline{RST}$ from 0 to 1)
- Change in FRQSEL, FRQTBL, BWSEL, or XTAL/CLOCK pins
- Internal DSPLL registers out-of-range, indicating the need to relock the DSPLL

In any of the above cases, an internal self-calibration will be initiated if a valid input clock exists (no input alarm) and is selected as the active clock at that time. The external crystal or reference clock must also be present for the self-calibration to begin. If valid clocks are not present, the self-calibration state machine will wait until they appear, at which time the calibration will start.

After a successful self-calibration has been performed with a valid input clock, no subsequent self calibrations are performed unless one of the above conditions are met. If the input clock is lost following self-calibration, the device enters holdover mode. When the input clock returns, the device relocks to the input clock without performing a self-calibration.

### 4.2.1. Input Clock Stability during Internal Self-Calibration

An exit from reset must occur when the selected CKINn clock is stable in frequency with a frequency value that is within the device operating range. The other CKINs must also either be stable in frequency or squelched during a reset.

### 4.2.2. Self-Calibration caused by Changes in Input Frequency

If the selected CKINn varies by 500 ppm or more in frequency since the last calibration, the device may initiate a self-calibration.

### 4.2.3. Device Reset

Upon powerup, the device internally executes a power-on-reset (POR) which resets the internal device logic. The pin $\overline{RST}$ can also be used to initiate a reset. The device stays in this state until a valid CKINn is present, when it then performs a PLL Self-Calibration (See 4.2. "PLL Self-Calibration”).

#### 4.2.4. Recommended Reset Guidelines

Follow the recommended RESET guidelines in Table 8 when reset should be applied to a device.

**Table 8. Si5315 Pins and Reset**

| Pin # | Si5315 Pin Name | Must Reset after Changing |
|---|---|---|
| 2 | FRQTBL | Yes |
| 11 | XTAL/CLOCK | Yes |
| 22 | BWSEL0 | Yes |
| 23 | BWSEL1 | Yes |
| 24 | FRQSEL0 | Yes |
| 25 | FRQSEL1 | Yes |
| 26 | FRQSEL2 | Yes |
| 27 | FRQSEL3 | Yes |

#### 4.2.5. Hitless Switching with Phase Build-Out

Silicon Laboratories switching technology performs "phase build-out" to minimize the propagation of phase transients to the clock outputs during input clock switching. All switching between input clocks occurs within the input multiplexor and phase detector circuitry. The phase detector circuitry continually monitors the phase difference between each input clock and the DSPLL output clock, $f_{OSC}$. The phase detector circuitry can lock to a clock signal at a specified phase offset relative to $f_{OSC}$ so that the phase offset is maintained by the PLL circuitry.

At the time a clock switch occurs, the phase detector circuitry knows both the input-to-output phase relationship for the original input clock and for the new input clock. The phase detector circuitry locks to the new input clock at the new clock's phase offset so that the phase of the output clock is not disturbed. The phase difference between the two input clocks is absorbed in the phase detector's offset value, rather than being propagated to the clock output.

The switching technology virtually eliminates the output clock phase transients traditionally associated with clock rearrangement (input clock switching). The Maximum Time Interval Error (MTIE) and maximum slope for clock output phase transients during clock switching are given in (Table 3, “AC Characteristics”). These values fall significantly below the limits specified in the ITU-T G.8262, Telcordia GR-1244-CORE, and GR-253-CORE requirements.

### 4.3. Input Clock Control

This section describes the clock selection capabilities (manual input selection, automatic input selection, hitless switching, and revertive switching). When switching between two clocks, LOL may temporarily go high if the two clocks differ in frequency by more than 100 ppm.

#### 4.3.1. Manual Clock Selection

Manual control of input clock selection is chosen via the CS_CA pin according to Table 9 and Table 10.

**Table 9. Automatic/Manual Clock Selection**

| AUTOSEL | Clock Selection Mode |
|---|---|
| L | Manual |
| M | Automatic non-revertive |
| H | Automatic revertive |

**Table 10. Manual Input Clock Selection, AUTOSEL = L**

| CS_CA | Si5315<br>AUTOSEL = L |
|---|---|
| 0 | CKIN1 |
| 1 | CKIN2 |

### 4.3.2. Automatic Clock Selection

The AUTOSEL input pin sets the input clock selection mode as shown in Table 9. Automatic switching is either revertive or non-revertive. Setting AUTOSEL to M or H, changes the CS_CA pin to an output pin that indicates the state of the automatic clock selection.

**Table 11. Clock Active Indicators, AUTOSEL = M or H**

| CS_CA | Active Clock |
|---|---|
| 0 | CKIN1 |
| 1 | CKIN2 |

The prioritization of clock inputs for automatic switching is shown in Table 12. This priority is hardwired in the devices.

**Table 12. Input Clock Priority for Auto Switching**

| Priority | Input Clocks |
|---|---|
| 1 | CKIN1 |
| 2 | CKIN2 |
| 3 | Holdover |

At power-on or reset, the valid CKINn with the highest priority (1 being the highest priority) is automatically selected. If no valid CKINn is available, the device suppresses the output clocks and waits for a valid CKINn signal.

If the currently selected CKINn goes into an alarm state, the next valid CKINn in priority order is selected. If no valid CKINn is available, the device enters holdover.

Operation in revertive and non- revertive is different when a signal becomes valid:

Revertive (AUTOSEL = H): The device constantly monitors all CKINn. If a CKINn with a higher priority than the current active CKINn becomes valid, the active CKINn is changed to the CKINn with the highest priority.

Non-revertive (AUTOSEL = M): The active clock does not change until there is an alarm on the active clock. The device will then select the highest priority CKINn that is valid. Once in holdover, the device will switch to the first CKINn that becomes valid.

## 4.4. Alarms

Summary alarms are available to indicate the overall status of the input signals. Alarm outputs stay high until all the alarm conditions for that alarm output are cleared.

### 4.4.1. Loss-of-Signal

The device has loss-of-signal circuitry that continuously monitors CKINn for missing pulses. The LOS circuitry generates an internal LOSn_INT output signal that is processed with other alarms to generate LOS1 and LOS2.

An LOS condition on CKIN1 causes the internal LOS1_INT alarm to become active. Similarly, an LOS condition on CKINn causes the LOSn_INT alarm to become active. Once a LOSn_INT alarm is asserted on one of the input clocks, it remains asserted until that input clock is validated over a designated time period. The time to clear LOSn_INT after a valid input clock appears is listed in Table 3, “AC Characteristics”. If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation time starts over.

#### 4.4.1.1. LOS Algorithm

The LOS circuitry divides down each input clock to produce an 8 kHz to 2 MHz signal. The LOS circuitry over samples this divided down input clock using a 40 MHz clock to search for extended periods of time without input clock transitions. If the LOS monitor detects twice the normal number of samples without a clock edge, a LOSn_INT alarm is declared. Table 3, “AC Characteristics” gives the minimum and maximum amount of time for the LOS monitor to trigger.

#### 4.4.1.2. Lock Detect

The PLL lock detection algorithm indicates the lock status on the LOL output pin. The algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. If the time between two consecutive phase cycle slips is greater than the retrigger time, the PLL is in lock. The LOL output has a guaranteed minimum pulse width as shown in (Table 3, “AC Characteristics”). The LOL pin is also held in the active state during an internal PLL calibration. The retrigger time is automatically set based on the PLL closed loop bandwidth (See Table 13).

**Table 13. Lock Detect Retrigger Time**

| PLL Bandwidth Setting (BW) | Retrigger Time (ms) |
|---|---|
| 60–120 Hz | 53 |
| 120–240 Hz | 26.5 |
| 240–480 Hz | 13.3 |
| 480–960 Hz | 6.6 |
| 960–1920 Hz | 3.3 |
| 1920–3840 Hz | 1.66 |
| 3840–7680 Hz | 0.833 |

## 4.5. Holdover Mode

If an LOS condition exists on the selected input clock, the device enters holdover. In this mode, the device provides a stable output frequency until the input clock returns and is validated. When the device enters holdover, the internal oscillator is initially held to its last frequency value. Next, the internal oscillator slowly transitions to a historical average frequency value that was taken over a time window of 6,711 ms in size that ended 26 ms before the device entered holdover. This frequency value is taken from an internal memory location that keeps a record of previous DSPLL frequency values. By using a historical average frequency, input clock phase and frequency transients that may occur immediately preceding loss of clock or any event causing holdover do not affect the holdover frequency. Also, noise related to input clock jitter or internal PLL jitter is minimized.

If a highly stable reference, such as an oven-controlled crystal oscillator, is supplied at XA/XB, an extremely stable holdover can be achieved. If a crystal is supplied at the XA/XB port, the holdover stability will be limited by the stability of the crystal; Table 3, “AC Characteristics” gives the specifications related to the holdover function.

### 4.5.1. Recovery from Holdover

When the input clock signal returns, the device transitions from holdover to the selected input clock. The device performs hitless recovery from holdover. The clock transition from holdover to the returned input clock includes "phase buildout" to absorb the phase difference between the holdover clock phase and the input clock phase. See Table 3, “AC Characteristics” for specifications.

## 4.6. PLL Bypass Mode

The Si5315 supports a PLL bypass mode in which the selected input clock is fed directly to both enabled output buffers, bypassing the DSPLL. Internally, the bypass path is implemented with high-speed differential signaling for low jitter. In PLL bypass mode, the input and output clocks will be at the same frequency. PLL bypass mode is useful in a laboratory environment to measure system performance with and without the jitter attenuation provided by the DSPLL. The DSBL2_BY pin is used to select the PLL Bypass Mode according to Table 14.

**Table 14. DSBL2/BYPASS Pin Settings**

| DSBL2/BYPASS | Function |
|---|---|
| L | CKOUT2 Enabled |
| M | CKOUT2 Disabled |
| H | PLL Bypass Mode w/ CKOUT2 Enabled |

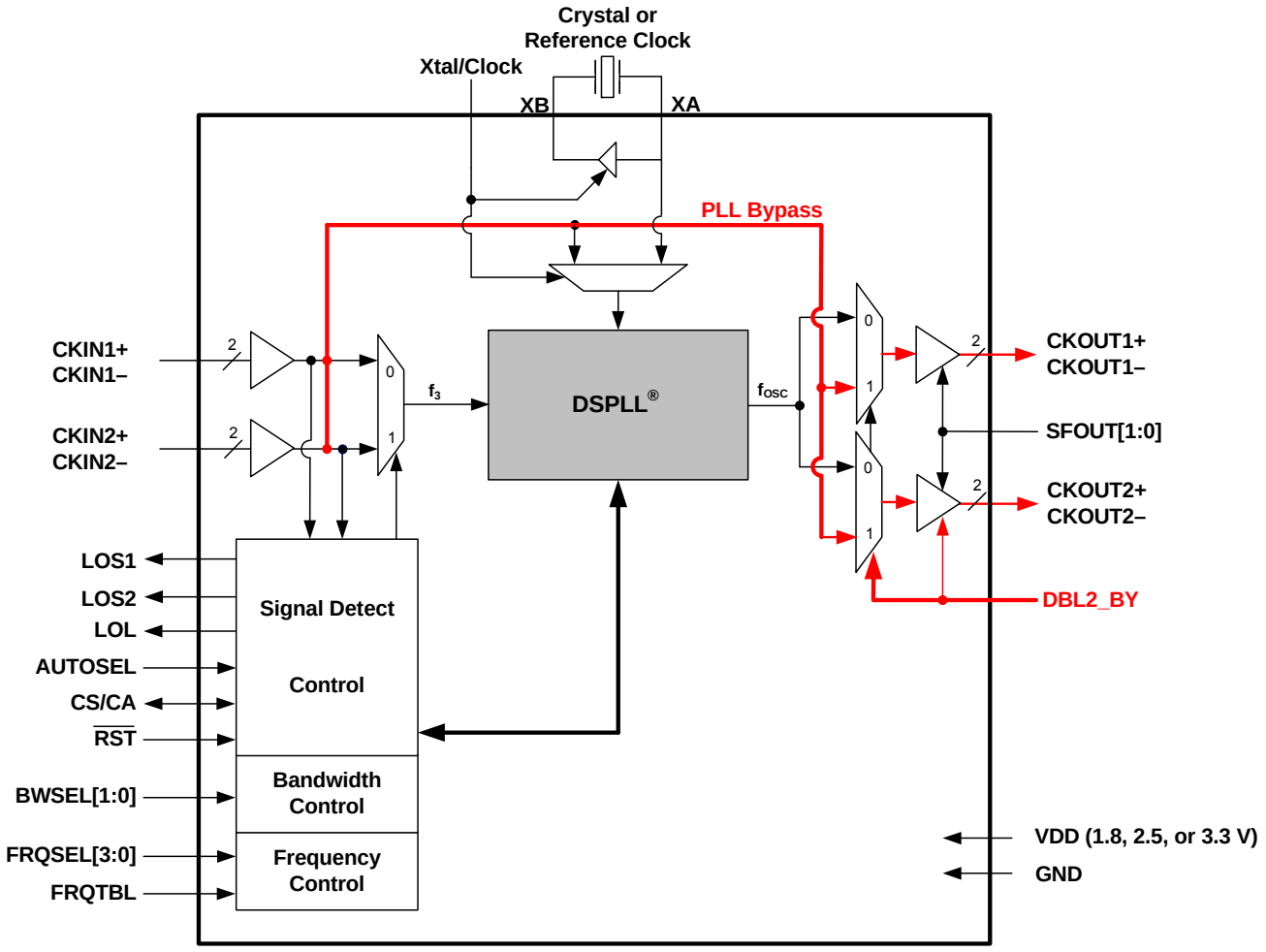



**Figure 9. Bypass Signal**

# 5. High-Speed I/O

## 5.1. Input Clock Buffers

The Si5315 provides differential inputs for the CKINn clock inputs. These inputs are internally biased to a common mode voltage [see Table 2, “DC Characteristics”] and can be driven by either a single-ended or differential source. Figure 10 through Figure 13 show typical interface circuits for LVPECL, CML, LVDS, or CMOS input clocks. Note that the jitter generation improves for higher levels on CKINn (within the limits in Table 3, “AC Characteristics”).

AC coupling the input clocks is recommended because it removes any issue with common mode input voltages. However, either ac or dc coupling is acceptable. Figures 10 and 11 show various examples of different input termination arrangements. Unused inputs can be left unconnected.

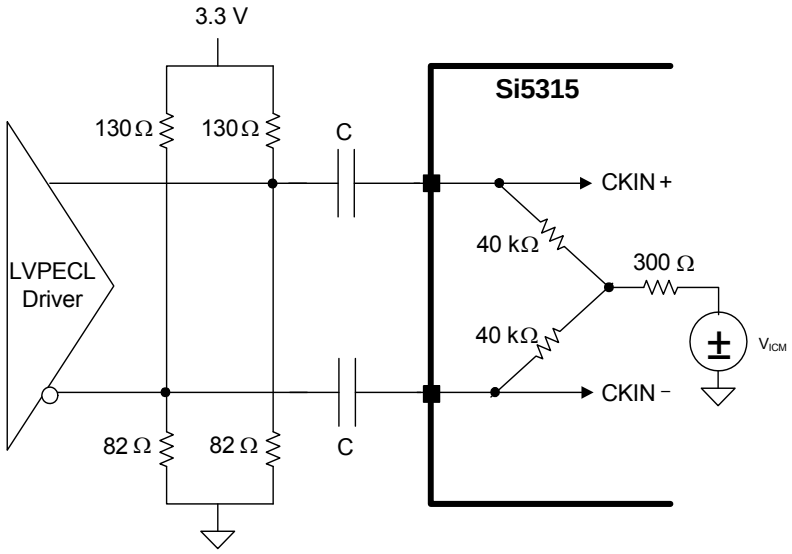



**Figure 10. Differential LVPECL Termination**

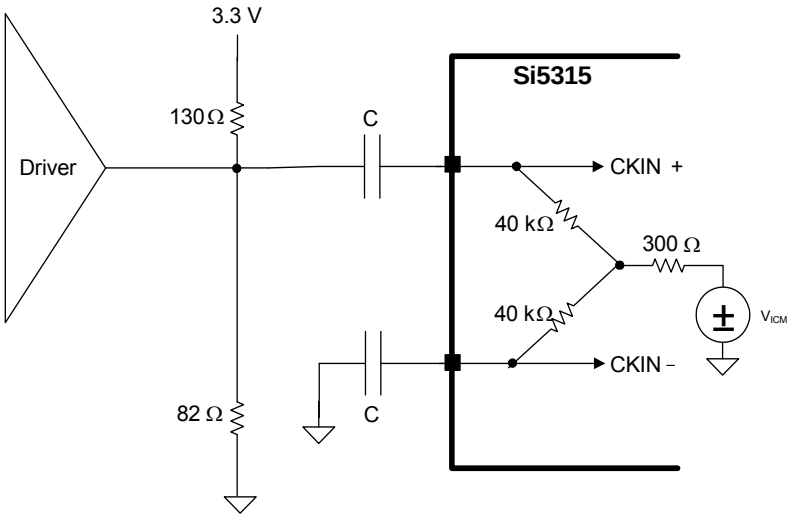



**Figure 11. Single-Ended LVPECL Termination**

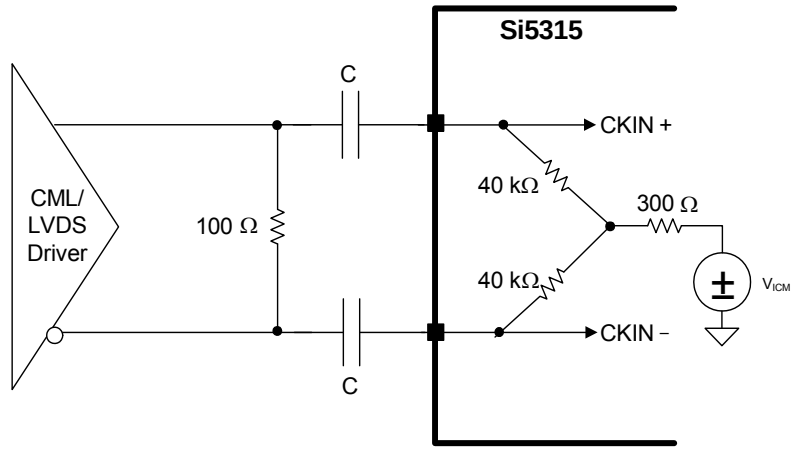



**Figure 12. CML/LVDS Termination (1.8, 2.5, 3.3 V)**

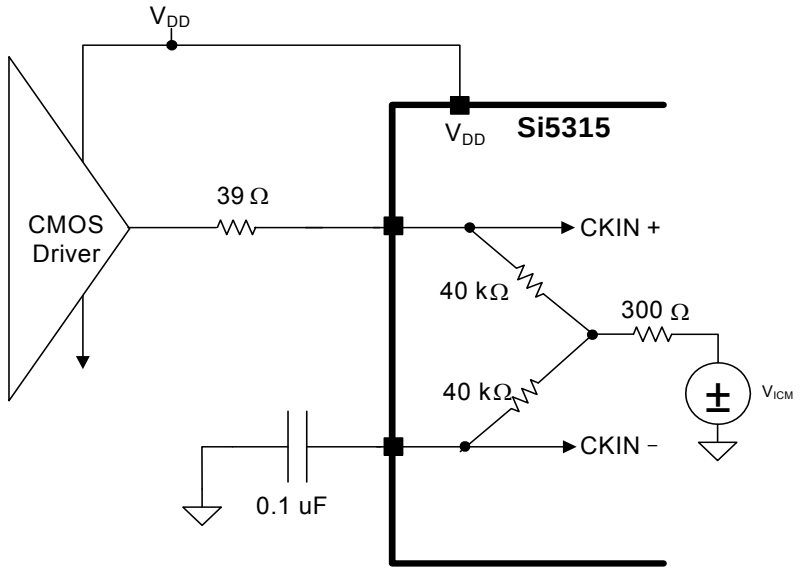



**Figure 13. CMOS Termination (1.8, 2.5, 3.3 V)**

## 5.2. Output Clock Drivers

The Si5315 has a flexible output driver structure that can drive a variety of loads, including LVPECL, LVDS, CML, and CMOS formats. The signal format is selected for both CKOUT1 and CKOUT2 outputs using the SFOUT [1:0] pins. This modifies the output common mode and differential signal swing. See Table 2, “DC Characteristics” for output driver specifications. The SFOUT [1:0] pins are three-level input pins, with the states designated as L (ground), M ($V_{DD}$/2), and H ($V_{DD}$). Table 15 shows the signal formats based on the supply voltage and the type of load being driven.

**Table 15. Output Signal Format Selection (SFOUT)**

| SFOUT[1:0] | Signal Format |
|---|---|
| HL | CML |
| HM | LVDS |
| LH | CMOS |
| LM | Disabled |
| MH | LVPECL |
| ML | Low-swing LVDS |
| All Others | Reserved |

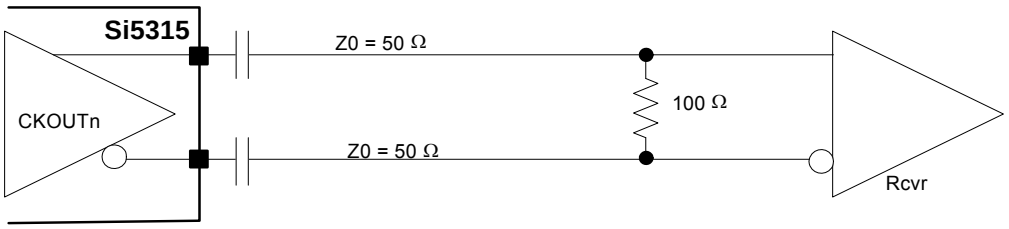



**Figure 14. Typical Differential Output Circuit**

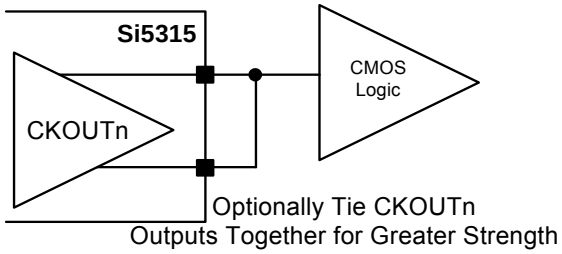



**Figure 15. Typical CMOS Output Circuit (Tie CKOUTn+ and CKOUTn– Together)**

For the CMOS setting (SFOUT = LH), both output pins drive single-ended in-phase signals and should be externally shorted together to obtain the drive strength specified in Table 2, “DC Characteristics”.

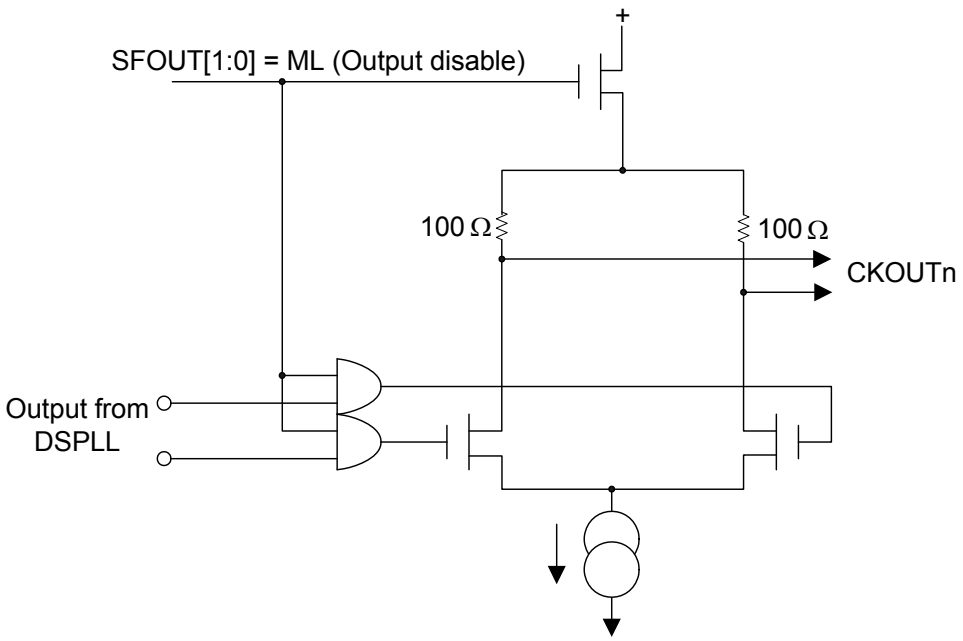



**Figure 16. CKOUTn Structure**

The SFOUT [1:0] pins can also be used to disable both outputs. Disabling the output puts the CKOUTn+ and CKOUTn– pins in a high-impedance state relative to $V_{DD}$ (common mode tri-state) while the two outputs remain connected to each other through a 200 Ω on-chip resistance (differential impedance of 200 Ω). The maximum amount of internal circuitry is powered down, minimizing power consumption and noise generation. Recovery from the disable mode requires additional time as specified in Table 3, “AC Characteristics”.

## 6. Crystal/Reference Clock Input

The device can use an external crystal or external clock as a reference. If an external clock is used, it must be ac coupled. With appropriate buffers, the same external reference clock can be applied to CKINn. Although the reference clock input can be driven single ended (See Figure 18), the best performance is with a crystal or differential clock source.

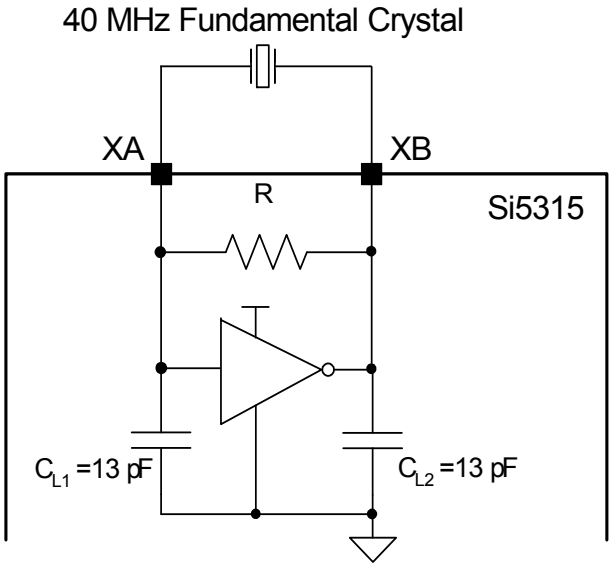
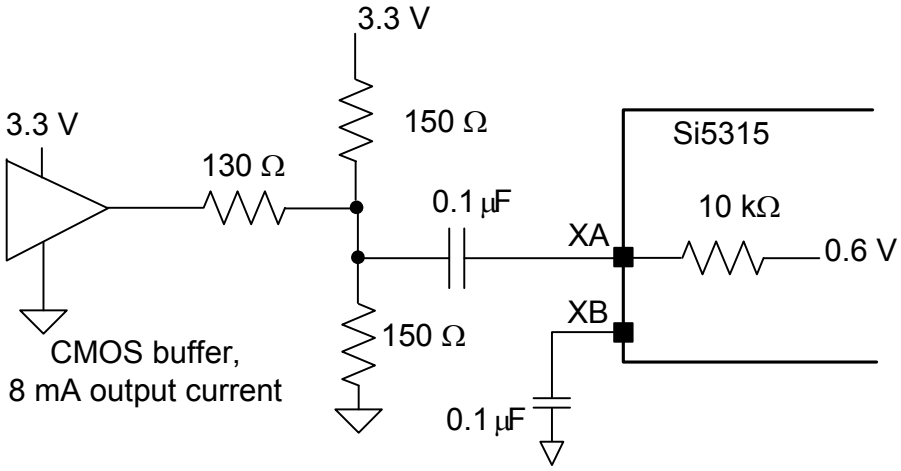



**Figure 17. Crystal Oscillator with Feedback Resistor**




For 2.5 V operation, change 130 Ω to 82 Ω.

**Figure 18. CMOS External Reference Circuit**

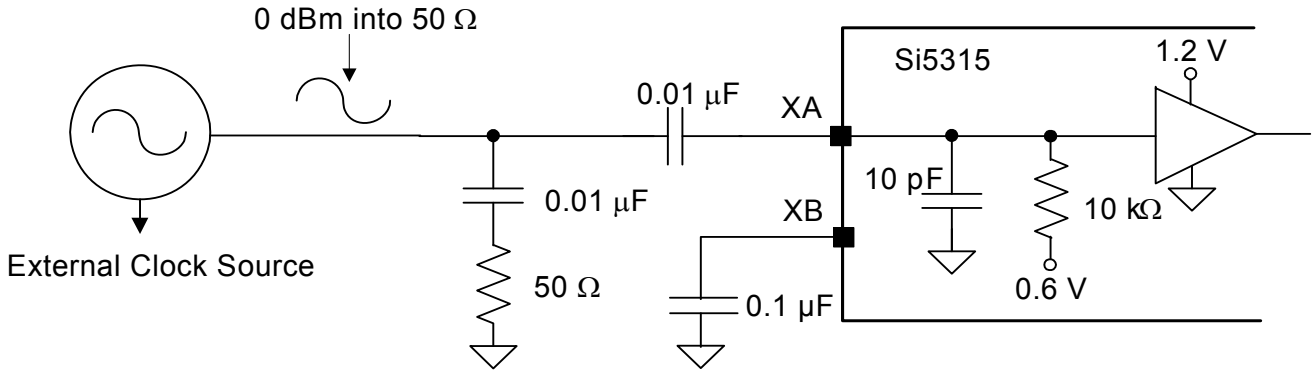



**Figure 19. Sinewave External Reference Clock Input Example**

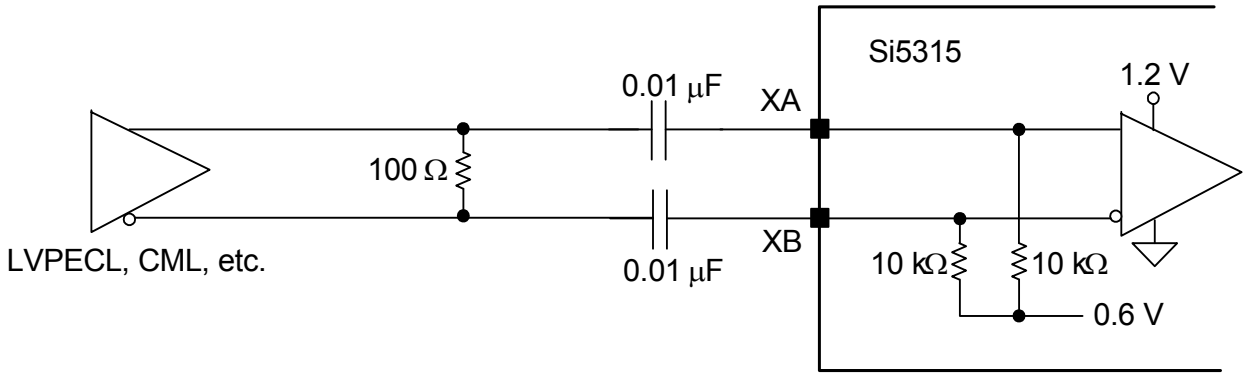



**Figure 20. Differential External Reference Clock Input Example**

## 6.1. Crystal/Reference Clock Selection

An external 40 MHz clock or a low-cost 40 MHz fundamental mode crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high-quality crystal.

In holdover, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in holdover will be tracked by the output of the device. Note that crystals can have temperature sensitivities. Table 16 shows the recommended 40 MHz fundamental mode crystals.

**Table 16. Recommended Crystals**

| Manufacturer | Part Number | Web Site |
|---|---|---|
| Abracon Corporation | ABM8-40.000MHZ-B2-T | http://www.abracon.com |
| Connor Winfield | XL-1CE | http://www.conwin.com |
| CTS Corporation | 403 | http://ctscorp.com |
| ECS Inc., International | ECS-400-20-33-A-S-L-TR | http://ecsxtal.com |
| Mtron | M1253-3-P-P-40.0000MHz | http://www.mtronpti.com |
| **Note:** While these crystals meet the preceding criteria according to their data sheets, Silicon Laboratories, Inc. does not guarantee operation with the Si5315, nor does Silicon Laboratories endorse one supplier of crystals over another. Contact Silicon Labs for details and a current list of crystal vendors and recommended part numbers. | | |

**Table 17. XA/XB Reference Sources**

| XTAL/CLOCK | Type |
|---|---|
| M | External clock |
| L | 40 MHz crystal |

Because the crystal is used as a jitter reference, rapid changes of the crystal temperature can temporarily disturb the output phase and frequency. For example, it is recommended that the crystal not be placed close to a fan that is being turned off and on. If a situation such as this is unavoidable, the crystal should be thermally isolated with an insulating cover.

### 6.1.1. Reference Drift

During holdover, long-term and temperature related drift of the reference input result in a one-to-one drift of the output frequency. That is, the stability of the any-rate output is identical to the drift of the reference frequency. This means that for the most demanding applications where the drift of a crystal is not acceptable, an external temperature compensated or ovenized oscillator will be required. Drift is not an issue unless the part is in holdover. Also, the initial accuracy of the reference oscillator (or crystal) is not relevant.

### 6.1.2. Reference Jitter

Jitter on the reference input has a roughly one-to-one transfer function to the output jitter over the bandwidth ranging from 100 Hz up to 30 kHz. If a crystal is used on the XA/XB pins, the reference will have low jitter if a suitable crystal is in use. If the XA/XB pins are connected to an external reference oscillator, the jitter of the external reference oscillator may contribute significantly to the output jitter.

## 7. Power Supply Filtering

This device incorporates an on-chip voltage regulator to power the device from supply voltages of 1.8, 2.5, or 3.3 V. Internal core circuitry is driven from the output of this regulator while I/O circuitry uses the external supply voltage directly. Table 3, “AC Characteristics” gives the sensitivity of the on-chip oscillator to changes in the supply voltage.

**The center ground pad under the device must be electrically and thermally connected to the ground plane. See Figure 25, “Ground Pad Recommended Layout,” on page 53.**

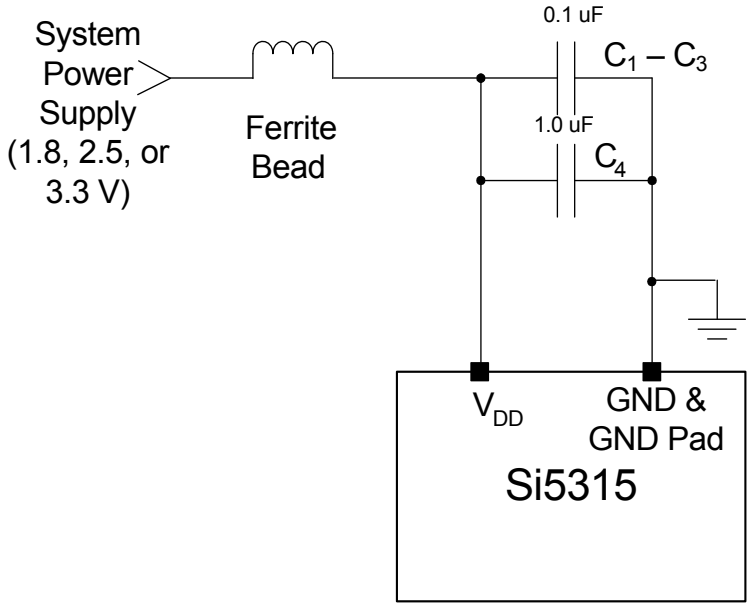
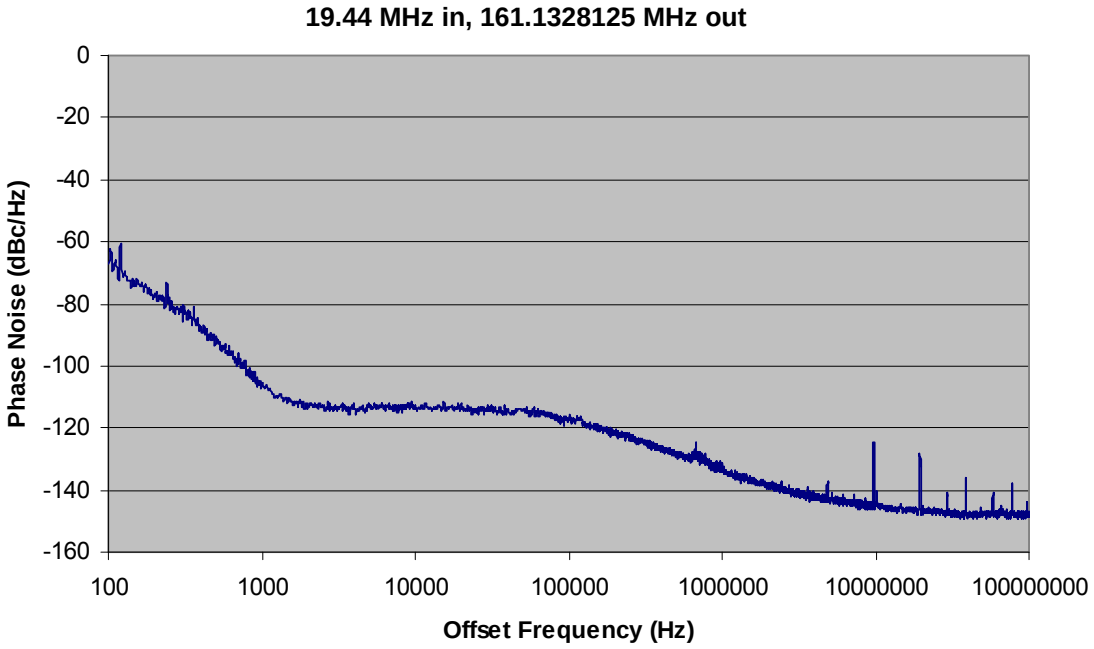



**Figure 21. Typical Power Supply Bypass Network**

# 8. Typical Phase Noise Plots

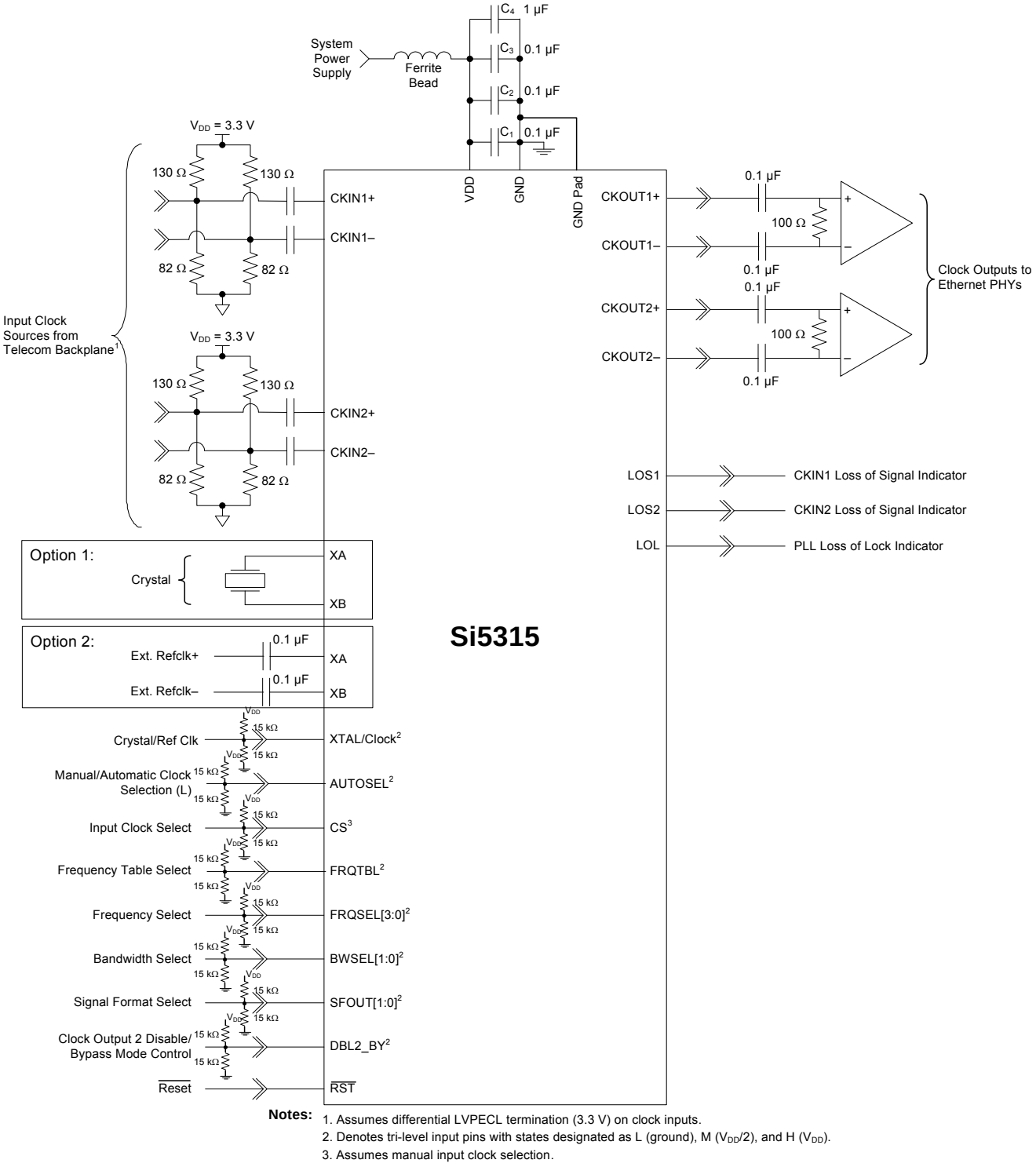
The following is a typical phase noise plot. The clock input source was a Rohde and Schwarz model SML03 RF Generator. The spectrum analyzer was either an Agilent model E4400A or an Agilent model JS-500. The Si5315 operates at 3.3 V with an ac coupled differential PECL output and an ac coupled differential sine wave input from the RF generator at 0 dBm. Note that, as with any PLL, the output jitter that is below the loop BW is caused by the jitter at the input clock, not the Si5315. Except as noted, loop BWs of 60 Hz to 100 Hz were in use.

## 8.1. Example: 10G LAN SyncE




| Jitter Band | Jitter, RMS |
|---|---|
| Brick Wall, 100 Hz to 100 MHz | TBD fs |
| SONET_OC48, 12 kHz to 20 MHz | TBD fs |
| SONET_OC192_A, 20 kHz to 80 MHz | TBD fs |
| SONET_OC192_B, 4 MHz to 80 MHz | TBD fs |
| SONET_OC192_C, 50 kHz to 80 MHz | TBD fs |
| Brick Wall,_800 Hz to 80 MHz | TBD fs |

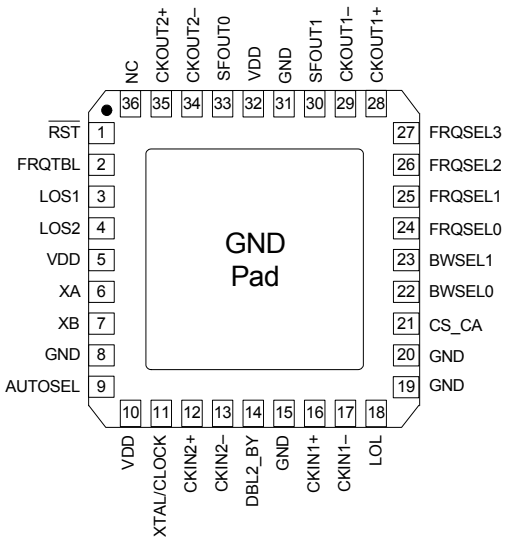
## 9. Typical Application Circuit




**Notes:**
1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M ($V_{DD}$/2), and H ($V_{DD}$).
3. Assumes manual input clock selection.

**Figure 22. Si5315 Typical Application Circuit**

## 10. Pin Descriptions: Si5315




Pin assignments are preliminary and subject to change.

**Table 18. Si5315 Pin Descriptions**

| Pin # | Pin Name | I/O | Signal Level | Description |
|---|---|---|---|---|
| 1 | $\overline{\text{RST}}$ | I | LVCMOS | **External Reset.**<br>Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5315 will perform an internal self-calibration when a valid input signal is present.<br>This pin has a weak pull-up. |
| 2 | FRQTBL | I | 3-Level | **Frequency Table Select.**<br>Selects frequency table. (Table 7 on page 21.)<br>Si5315A supports L/M/H.<br>Si5315B supports only L/M for normal operation.<br>H is reserved.<br>This pin has a weak pull-up and weak pull-down and defaults to M.<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. |
| 3 | LOS1 | O | LVCMOS | **CKIN1 Loss of Signal.**<br>Active high loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated.<br>0 = CKIN1 present<br>1 = LOS on CKIN1 |
| 4 | LOS2 | O | LVCMOS | **CKIN2 Loss of Signal.**<br>Active high loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated.<br>0 = CKIN2 present<br>1 = LOS on CKIN2 |

**Table 18. Si5315 Pin Descriptions (Continued)**

| Pin # | Pin Name | I/O | Signal Level | Description |
|---|---|---|---|---|
| 5, 10, 32 | $V_{DD}$ | $V_{DD}$ | Supply | **Supply.**<br>The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following $V_{DD}$ pins:<br>5 0.1 µF<br>10 0.1 µF<br>32 0.1 µF<br>A 1.0 µF should also be placed as close to device as is practical. |
| 7<br>6 | XB<br>XA | I | Analog | **External Crystal or Reference Clock.**<br>External crystal should be connected to these pins to use internal oscillator based reference. Crystal or reference clock selection is set by the XTAL/CLOCK pin. |
| 8, 15,19, 20,31 | GND | GND | Supply | **Ground.**<br>Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device. |
| 9 | AUTOSEL | I | 3-Level | **Manual/Automatic Clock Selection.**<br>Three level input that selects the method of input clock selection to be used.<br>L = Manual<br>M = Automatic non-revertive<br>H = Automatic revertive<br>This pin has a weak pull-up and weak pull-down and defaults to M.<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. |
| 11 | XTAL/CLOCK | I | 3-Level | **External Crystal or Reference Clock Rate.**<br>Three level input that selects the type and rate of external crystal or reference clock to be applied to the XA/XB port. This pin has both a weak pull-up and a weak pull-down and defaults to M.<br>L = Crystal<br>M = Clock (Default)<br>H = Reserved<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. |
| 12<br>13 | CKIN2+<br>CKIN2– | I | | **Clock Input 2.**<br>Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2. |

**Table 18. Si5315 Pin Descriptions (Continued)**

| Pin # | Pin Name | I/O | Signal Level | Description |
|---|---|---|---|---|
| 14 | DBL2_BY | I | 3-Level | **Output 2 Disable/Bypass Mode Control.**<br>Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode.<br>L = CKOUT2 enabled<br>M = CKOUT2 disabled<br>H = Bypass mode with CKOUT2 enabled<br>This pin has a weak pull-up and weak pull-down and defaults to M.<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. |
| 16<br>17 | CKIN1+<br>CKIN1– | I | Multi | **Clock Input 1.**<br>Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2. |
| 18 | LOL | O | LVCMOS | **PLL Loss of Lock Indicator.**<br>This pin functions as the active high PLL loss of lock indicator.<br>0 = PLL locked<br>1 = PLL unlocked |
| 21 | CS_CA | I/O | LVCMOS | **Input Clock Select/Active Clock Indicator.**<br>**Input**: If manual clock selection mode is chosen (AUTOSEL = L), this pin functions as the manual input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CS input state.<br>0 = Select CKIN1<br>1 = Select CKIN2<br>If configured as input, must be set high or low.<br>**Output**: If automatic clock selection mode is chosen (AUTOSEL = M or H), this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both CKIN1 and CKIN2, indicating that the holdover state has been entered, CA will indicate the last active clock that was used before entering the hold state.<br>0 = CKIN1 active input clock<br>1 = CKIN2 active input clock |
| 23<br>22 | BWSEL1<br>BWSEL0 | I | 3-Level | **Loop Bandwidth Select.**<br>Three level inputs that select the DSPLL closed loop bandwidth. See Table 7 on page 21 for available settings.<br>These pins have both weak pull-ups and weak pull-downs and default to M.<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. |

**Table 18. Si5315 Pin Descriptions (Continued)**

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>27<br>26<br>25<br>24</td><td>FRQSEL3<br>FRQSEL2<br>FRQSEL1<br>FRQSEL0</td><td>I</td><td>3-Level</td><td>Frequency Select.<br>Three level inputs that select the input clock and clock multiplication ratio, depending on the FRQTBL setting.<br>These pins have both weak pull-ups and weak pull-downs and default to M.<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</td></tr>
<tr><td>29<br>28</td><td>CKOUT1–<br>CKOUT1+</td><td>O</td><td>Multi</td><td>Clock Output 1.<br>Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>33<br>30</td><td>SFOUT0<br>SFOUT1</td><td>I</td><td>3-Level</td><td>Signal Format Select.<br>Three level inputs that select the output signal format (common mode voltage and differential swing) for both CKOUT1 and CKOUT2.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>LVDS</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS—Low Swing</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Disable</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table>
These pins have both weak pull-ups and weak pull-downs and default to M.<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</td></tr>
<tr><td>34<br>35</td><td>CKOUT2–<br>CKOUT2+</td><td>O</td><td>Multi</td><td>Clock Output 2.<br>Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>36</td><td>NC</td><td>—</td><td>—</td><td>No Connect.<br>Leave floating. Make no external connections to this pin for normal operation.</td></tr>
<tr><td>GND<br>PAD</td><td>GND</td><td>GND</td><td>Supply</td><td>Ground Pad.<br>The ground pad must provide a low thermal and electrical impedance to a ground plane.</td></tr>
</table>

## 11. Ordering Guide

| Ordering Part Number | Output Clock Freq Range | Pkg | ROHS6, Pb-Free | Temp Range |
|---|---|---|---|---|
| Si5315A-C-GM | 8 kHz–644.53 MHz | 36-Lead 6x6 mm QFN | Yes | –40 to 85 °C |
| Si5315B-C-GM | 8 kHz–125 MHz | 36-Lead 6x6 mm QFN | Yes | –40 to 85 °C |
| **Note:** Add an R at the end of the device to denote tape and reel options (i.e., Si5315A-C-GMR). | | | | |

**Table 19. Product Selection Guide**

| Device | Clock Inputs | Clock Outputs | µP Control | Max Input Freq (MHz)[1] | Max Output Frequency (MHz) | Jitter Generation (12 kHz – 20 MHz) | Hitless Switching | LOS Alarm | LOL Alarm | FOS Alarm | FSYNC Realignment |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Any-Rate Precision Clock Multipliers (Wideband)** | | | | | | | | | | | |
| Si5322 | 2 | 2 | | 707 | 1050 | 0.6 ps rms typ | | ● | | | |
| Si5325 | 2 | 2 | ● | 710 | 1400 | 0.6 ps rms typ | | ● | | ● | |
| Si5365 | 4 | 5 | | 707 | 1050 | 0.6 ps rms typ | | ● | | ● | |
| Si5367 | 4 | 5 | ● | 710 | 1400 | 0.6 ps rms typ | | ● | | ● | |
| **Any-Rate Precision Clock Multipliers w/Jitter Attenuation[2] (Narrowband)** | | | | | | | | | | | |
| Si5315[2] | 2 | 2 | | 644 | 644 | 0.6 ps rms typ | ● | ● | ● | | |
| Si5316[3] | 2 | 1 | | 707 | 710 | 0.3 ps rms typ | | ● | ● | | |
| Si5319[3] | 1 | 1 | ● | 710 | 1400 | 0.3 ps rms typ | | ● | ● | | |
| Si5323[3] | 2 | 2 | | 707 | 1050 | 0.3 ps rms typ | ● | ● | ● | | |
| Si5326[3] | 2 | 2 | ● | 710 | 1400 | 0.3 ps rms typ | ● | ● | ● | ● | |
| Si5366[3] | 4 | 5 | | 707 | 1050 | 0.3 ps rms typ | ● | ● | ● | ● | ● |
| Si5368[3] | 4 | 5 | ● | 710 | 1400 | 0.3 ps rms typ | ● | ● | ● | ● | ● |

**Notes:**
1. Maximum input and output rates may be limited by speed rating of device. See each device's data sheet for ordering information.
2. Requires external low-cost, fixed frequency fundamental mode 40 MHz crystal or reference clock. See Table 17 on page 43.
3. Requires external low-cost, fixed frequency 3rd overtone 114.285 MHz crystal or reference clock. See the Family Reference Manual for more details.

## 12. Package Outline: 36-Pin QFN

Figure 23 illustrates the package details for the Si5315. Table 20 lists the values for the dimensions shown in the illustration.

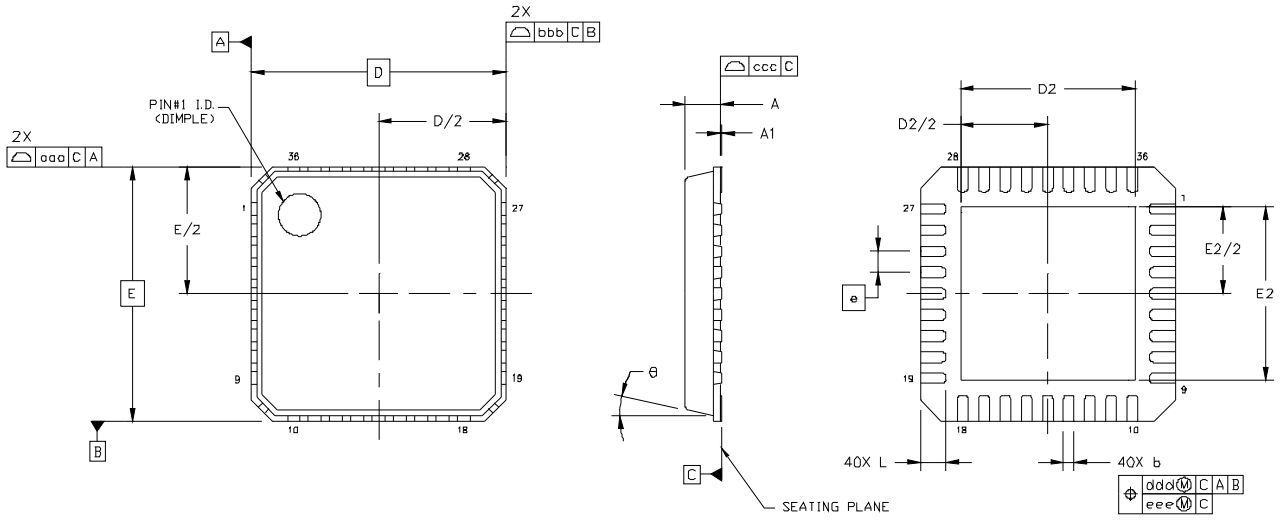



**Figure 23. 36-Pin Quad Flat No-Lead (QFN)**

**Table 20. Package Dimensions**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | | 6.00 BSC | |
| D2 | 3.95 | 4.10 | 4.25 |
| e | | 0.50 BSC | |
| E | | 6.00 BSC | |
| E2 | 3.95 | 4.10 | 4.25 |

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| L | 0.50 | 0.60 | 0.70 |
| θ | — | — | 12º |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.05 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 13. Recommended PCB Layout

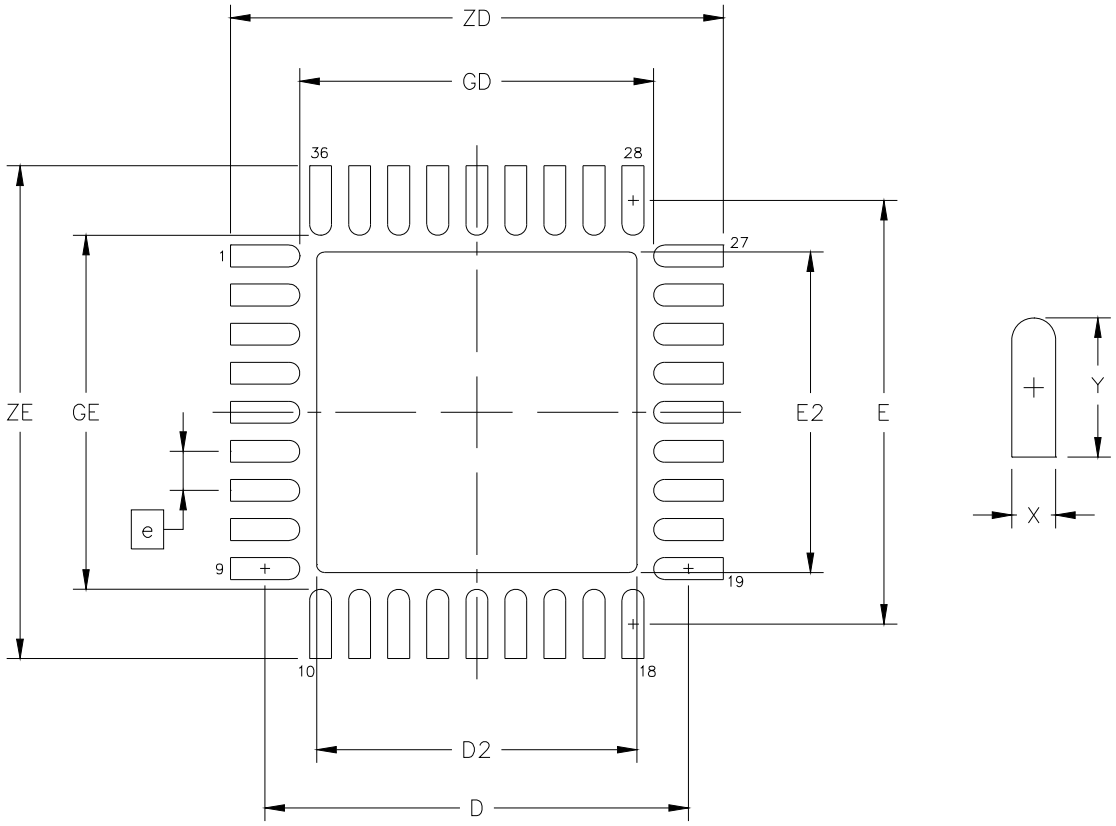



**Figure 24. PCB Land Pattern Diagram**

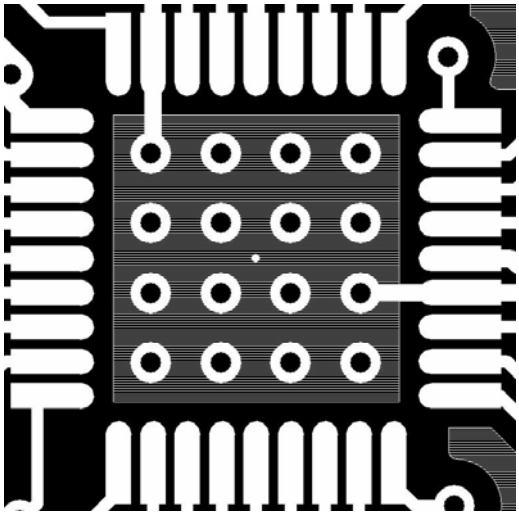


**Figure 25. Ground Pad Recommended Layout**

**Table 21. PCB Land Pattern Dimensions**

| Dimension | MIN | MAX |
|---|---|---|
| e | 0.50 BSC. | |
| E | 5.42 REF. | |
| D | 5.42 REF. | |
| E2 | 4.00 | 4.20 |
| D2 | 4.00 | 4.20 |
| GE | 4.53 | — |
| GD | 4.53 | — |
| X | — | 0.28 |
| Y | 0.89 REF. | |
| ZE | — | 6.31 |
| ZD | — | 6.31 |

**Notes (General):**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Notes (Solder Mask Design):**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

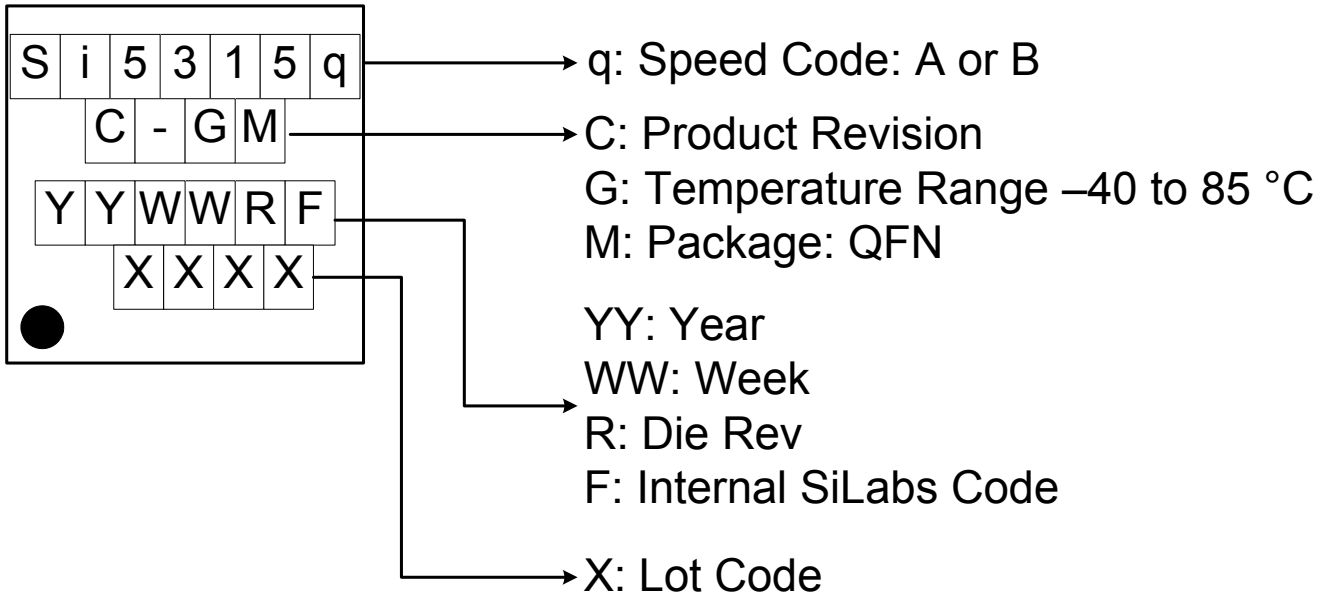
**Notes (Stencil Design):**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

**Notes (Card Assembly):**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 14. Si5315 Device Top Mark


S i 5 3 1 5 q
C - G M
Y Y W W R F
X X X X
q: Speed Code: A or B
C: Product Revision
G: Temperature Range –40 to 85 °C
M: Package: QFN
YY: Year
WW: Week
R: Die Rev
F: Internal SiLabs Code
X: Lot Code

## CONTACT INFORMATION

**Silicon Laboratories Inc.**

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: Clockinfo@silabs.com
Internet: www.silabs.com

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